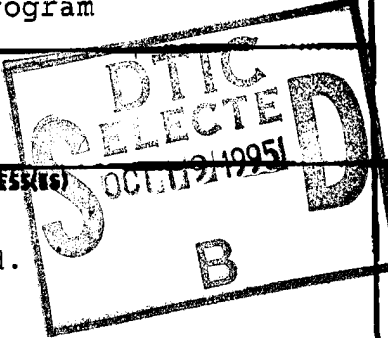# REPORT DOCUMENTATION PAGE

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The thrust of this program has been to perform research and development at AET, Inc. and Florida Institute of Technology (Florida Tech) aimed at transforming the STADIUM technology into a user-friendly tool for both military and commercial applications. The overall technical objective of the program has been to establish the feasibility of statistical semiconductor device simulation based on the methodology of design of experiments for the Low Power Electronics Program. In addition, we have investigated methodologies for developing statistical process, device and circuit models for silicon-on-insulator technologies which can be used to optimize wafer tab processes and devices and to determine critical process operations for yield optimization. These capabilities will lead to reductions of manufacturing costs and time-to-market and an increase in product reliability.

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Statistical Modeling of SOI Devices for the Low Power Electronics Program

Final Report for
Phase I SBIR Program

ARPA Contract No.
DAAH01-95-C-R031

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September 6, 1995

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Advanced Engineering
Technology

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STATISTICAL MODELING OF SOI DEVICES
FOR THE
LOW POWER ELECTRONICS PROGRAM

Final Report

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STATISTICAL MODELING OF SOI DEVICES FOR THE LOW POWER ELECTRONICS PROGRAM

Final Report

1. Introduction

The thrust of this program has been to perform research and development at AET, Inc. and Florida Institute of Technology (Florida Tech) aimed at transforming the STADIUM technology into a user-friendly tool for both military and commercial applications. The overall technical objective of the program has been to establish the feasibility of statistical semiconductor device simulation based on the methodology of design of experiments for the Low Power Electronics program. In addition, we have investigated methodologies for developing statistical process, device and circuit models for silicon-on-insulator technologies which can be used to optimize wafer fab processes and devices and to determine critical process operations for yield optimization. These capabilities will lead to reductions of manufacturing costs and time-to-market and an increase in product reliability. The results are applicable to both military and industrial environments giving true dual use products. The specific objectives which have been achieved during the program are:

1. Completed development of a comprehensive program plan which is in concert with the US government and DOD contractor needs and plans. This included a visit early in the program to ARPA to verify the program objectives.

2. Specified program changes needed in the STADIUM software which was developed under SEMATECH funding. A prototype software package called STADIUM™SOI has been developed. The objective has been a user-friendly tool whereby an engineer can apply design of experiments to silicon-on-insulator device simulations. This has achieved the desired result of estimating product variations as a function of manufacturing variations.

3. Identified methodology for applying design of experiments to circuit simulation using the commercial PSpice program. A prototype software program has been written which clearly demonstrates the capability to achieve statistical circuit results. Although this software is not being delivered as part of this SBIR contract, a complete description of the development work is given in this report.

4. Developed partnerships with Lincoln Labs and SEMATECH for developing statistical model parameters for the silicon-on-insulator devices. The statistical models are based upon process variations. These models can be used by integrated circuit designers in the synthesis of new processes and optimization of existing processes for technology and product-specific applications.

5. Studied optimization techniques including Taguchi and response surface methods so that a manufacturable process can be developed and optimized. This includes computerization of the design of experiments methodology so that it can be easily used by the integrated circuit designers.

6. Completed a Quarterly Report, this detailed Final Report and a proposal to commercialize the STADIUM technology in a Phase II SBIR program.

1.1 Deliverables

The significant results which AET has delivered as part of this Phase I SBIR contract include:

1. **STADIUM™SOI.** A proof-of-concept version of STADIUM (called STADIUM™SOI) has been completed which can be used for statistical simulation of silicon-on-insulator devices employing SUPREM and PISCES type simulators. STADIUM™SOI was delivered on schedule to the ARPA Program Manager, Zachary Lemnios, an August 4, 1995. Details of this software development work are given in sections 3, 4 and 5 of this report.

2. **Technology Transfer and SOI Statistical Models.** Partnerships were developed with Lincoln Labs, SEMATECH and other organizations. Some of these partnerships have resulted in the generation of statistical silicon-on-insulator device models. Details of these partnerships are given in section 6 of this report.

3. **Optimization Methodology.** Concepts for utilizing design of experiments based optimization techniques in silicon-on-insulator integrated circuit designs have been developed. Details of this research are given in section 7 of this report.

    Documentation and Reports. All documentation and reports were delivered on schedule. These include the Program Plan, the Quarterly Report, the STADIUM™SOI software and manual, and this Final Report.

1.2 Project Schedule

This project was set-up as a 7 month program with the schedule shown in Figure 1.
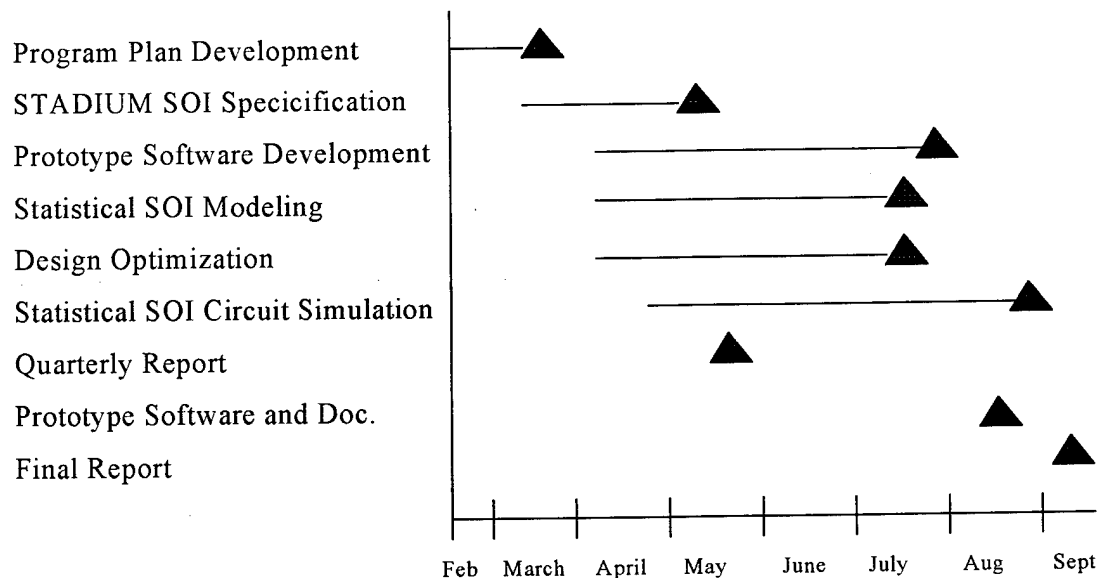
Figure 1. Statistical Modeling of SOI Devices for the Low Power Electronics Program Plan

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1.3 Report Outline

The remaining sections of this report present the following information:

- Section 2. Background information on the benefits of statistical simulation and prior research performed at Florida Tech.
- Section 3. Software design considerations for a new implementation of the STADIUM methodology especially suited to SOI processes.
- Section 4. STADIUM™SOI software description and windows menu system.
- Section 5. Description of statistical circuit simulation methods.
- Section 6. Statistical SOI modeling issues, techniques and industrial interactions.
- Section 7. Optimization techniques which may be applied to STADIUM.
- Section 8. Other program activities.
- Section 9. Conclusions developed from this PhaseI program.
- Section 10. Bibliography
- Appendices

2. STADIUM Statistical Simulation Methodology

2.1 STADIUM Background

Research and development of the STADIUM methodology and software began over four years ago at Florida Tech. While much of this work was performed under the Florida SEMATECH Center of Excellence program managed by SRC, research at Florida Tech now continues through direct contracts with SEMATECH and Texas Instruments. The STADIUM system is intended to be used with existing simulators (e.g., SUPREM-4, PISCES-2B and SPICE) for statistical process, device and circuit design. The 1993 SEMATECH Accomplishments Report lists STADIUM as one of three significant results coming out of the eleven SRC managed SEMATECH Centers of Excellence. This section describes some of the features of STADIUM.

The methodology developed for this SEMATECH research includes the integration of commercially available process, device and circuit simulators and statistical analysis tools with new software developed at Florida Tech. Emphasis has been placed on reducing the total number of simulation runs required while still maintaining statistically valid results. A design of experiments statistical methodology has been employed. The statistical simulation methodology implemented in STADIUM is illustrated in Figure 2. Both circuit parametric variations and defect yield estimates are determined as a function of measurements made in manufacturing. In this simulation flow, process and equipment variations are used as the input for statistical process design. The resulting estimated process variations are used as the input for statistical device design. The resulting estimated device variations are used as the input for statistical circuit design which can be combined with defect models to give accurate predictions of overall yield. The result is a product that works the first time, has high manufacturing yield and has a greatly reduced product to market cycle time.
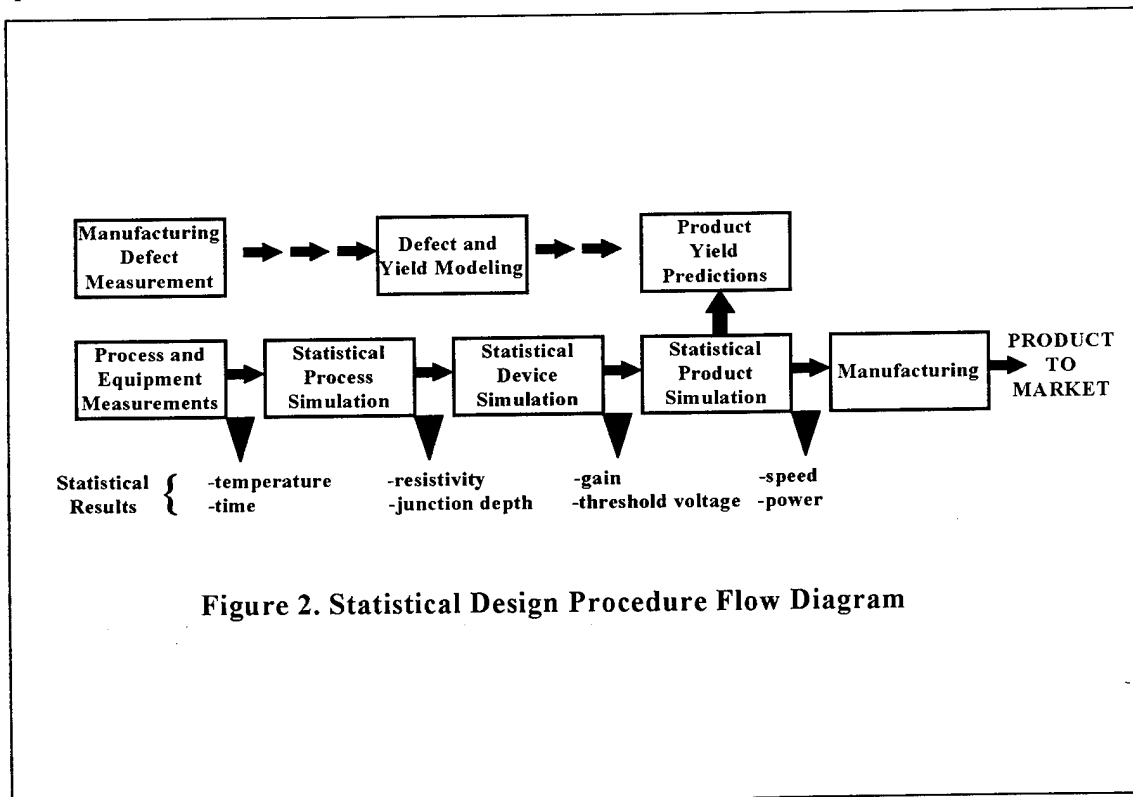

Figure 2. Statistical Design Procedure Flow Diagram

STADIUM provides a menu-driven windows user interface that allows for specification of CMOS and bipolar processes, known manufacturing variables, and device and circuit operation parameters independent of the simulators to be employed. Using this data and automated design of experiments techniques, batches of simulations are run and statistically analyzed to ultimately predict circuit performance, variability and yield.

2.2 STADIUM Statistical Simulation Methodology

The National Research Council, sponsored by the National Science Foundation, developed a report titled, Improving Engineering Design. This report concludes that "efficient engineering design can improve quality, reduce costs and speed time to market, thereby better matching products to customer needs. Effective design is also prerequisite for effective manufacturing." The Research Council Report further defines this methodology as one that fully integrates statistical "practices (such as Taguchi methods) and tools (such as CAD and CAE)." This integration of statistical practices and simulation tools is one of the primary goals for our research.

In the manufacturing sciences, it is important that simulators be used to help describe the relationship between product design and the manufacturing process to the product's final characteristics. Simulators facilitate proper design and manufacturing of products. Equally important are the effects of uncontrollable variation in the manufacturing parameters on the end product. If the product's characteristics are sensitive to slight variations in the manufacturing process, the yield or percentage of marketable units produced may decrease. Furthermore, understanding the sensitivity of the product characteristics can help in the design of more reliable products and increase the overall quality of the product.

Monte Carlo methods, because of their simplicity, have often been used to predict the impact of manufacturing variations. However, Monte Carlo based methods suffer from a number of related difficulties. A large number of simulation runs are needed to obtain an accurate yield estimate. Furthermore, Monte Carlo methods do not provide any vital information such as how the response varies as a function of input variables, which are the most significant input variables, or how can the response be optimized.

Conversely, a carefully planned approach to conduct a designed experiment (i.e., a design of experiments) can give valid answers to these questions while maintaining a low cost (number of simulation runs) for the experiment. The statistical methodology called design of experiments has long been used in manufacturing process development. It is used as a systematic way of optimizing a process while minimizing the number of replications needed to achieve that optimization. STADIUM implements this design of experiments methodology in a simulation mode as described in later paragraphs.

There are additional reasons why this statistical methodology has not been used in systems design. The primary one is that although design of experiments can be used to estimate the mean and standard deviation of the output response, it has been practiced only by statisticians. It involves a complex mathematical manipulation that can be best managed via computer solutions. STADIUM includes software modules that guide the engineer through this complex mathematical sequence.

Another obstacle overcome by STADIUM and its implementation of design of experiments involves the difficulties encountered in running the simulators. Many simulators require the engineer to have considerable detail knowledge about both the manufacturing processes and the internal workings of the simulators themselves. STADIUM includes a user-friendly, menu-driven input system where the engineer can easily enter the specifics of the system, and the software automatically sets up the simulations and runs them with the proper input variables as dictated by the specific design of experiments.

As shown in Figure 3, the statistical design for manufacturing methodology developed and implemented via STADIUM makes it possible to characterize responses as a function of manufacturing variables (e.g., ion implantation dose) at each level of simulation (process, device and circuit). The present version of STADIUM completed by Florida Tech allows for specification of CMOS and bipolar process and device parameters, design of experiments, automated running of batches of simulations, and includes interfacing to RS1/E/D statistical tools and on-line guidance for statistical analysis. It also includes an initial capability for performing statistical circuit simulation and analysis.

STADIUM has been designed to be a very versatile software system. One of its strengths is illustrated in Figure 3. Here it is clear that the design engineer can enter the IC simulation process at any point and still achieve valid statistical results. Specifically, the design system flow can be entered at the process simulation level, the device simulation level or at circuit simulation. The only constraint is the ability to generate appropriate statistical models at the point of entry.
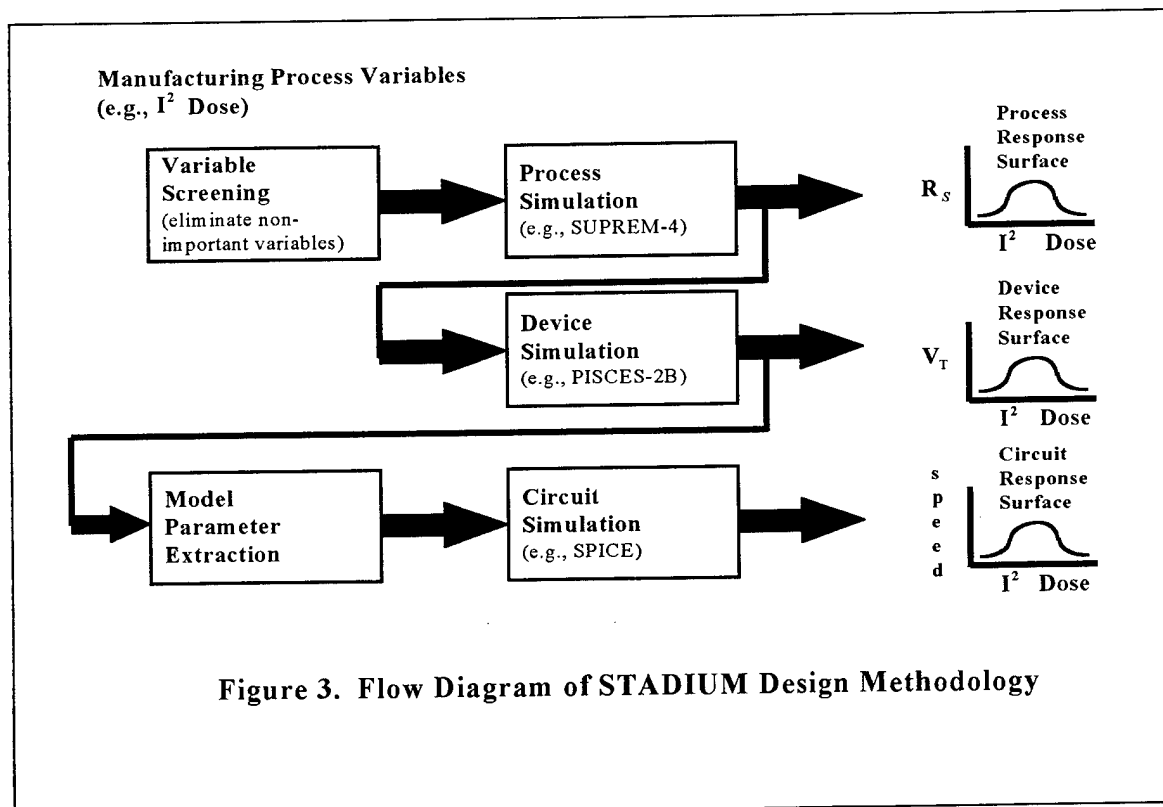

Figure 3. Flow Diagram of STADIUM Design Methodology

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STADIUM's generic process specification employs a hierarchical approach where libraries of objects (i.e., implants, oxidations, etc.) and macros (groups of objects) are created using pop-up menus. A similar menu then allows for the building of flows using objects and macros from these libraries. Specific attributes, values and optionally, standard deviations are specified when objects are created and edited. When a variable (temperature, implant dose, etc.) is specified along with a standard deviation, it will automatically be treated as an input factor by the design of experiments module within STADIUM. The flow is designed and captured independent of the process simulator to be used. Simulator specific information is either automatically generated or input via a simulator specific menu when interpreter modules specific to each simulator are activated during creation of input files for the simulator.

The design of experiments methodology allows the user to specify a single experiment containing both process and device variables. The final structures created by the process simulator (SUPREM-4) are used as input to the device simulator (PISCES-2B) for definition of doping profiles and topology information. Important process variables can be specified with nominal values and standard deviations. Other process parameters can be set to fixed values. It is also possible to set some device parameters as variables. If the user has chosen to do a device simulation and has also provided variations for one or more of these variables, then STADIUM can create a design of experiments that includes these and any process level variations specified.

Once an experimental design has been specified, an appropriate design file is generated by STADIUM to be used by the Multiple Simulation Controller (MSC) program. The design file contains the sigma variations to be used for each run in the current experiment. These sigma values are combined with the mean and standard deviations for the associated variables, and the results are substituted into the appropriate template. The template is then run with the simulator chosen, and the simulation results are saved.

Following the running of a batch of simulations, selected outputs are automatically extracted for each run and then merged with the design of experiments matrix of input variables to form a table ready for submission to the statistical analysis routines for regression analysis. STADIUM then provides menu-driven guidelines that help the engineer perform a valid statistical analysis and ultimately generate a model for each response from which estimates of the mean, variance and contribution of each input factor to the variance can be obtained.

The Florida Tech research has concentrated on coupling more efficient statistical techniques, based on a design of experiments methodology and conventional simulators, to characterize circuit performances in terms of equipment and material variables. The STADIUM methodology is well suited for a design for manufacturing (DFM) system that aims at predicting process yields and optimizing manufacturing processes before actual production, or at improving existing processes with the intent of increasing yield and lowering production costs.

STADIUM supplies the statistical knowledge and capability to the engineer which have in the past hindered implementation of design of experiments in a simulation environment. It has long been recognized that statistical simulation is a desirable methodology and necessary to achieve a deep understanding of the naturally occurring variations found in any system. Only through the use of statistical design techniques will the engineer have confidence that the system will perform as specified under all conditions.

3. Software Design Overview

STADIUM-SOI is a Technology-Computer-Aided-Design (TCAD) tool that combines the field of statistics with Silicon-On-Insulator (SOI) Integrated Circuit (IC) design. Computer simulation has the potential to improve IC chip yields only if the software is practical to use. STADIUM-SOI improves upon current commercial simulator packages by providing an improved easy-to-use interface (shell) and automated statistical design and analysis capabilities. This statistical system allows engineers to supplement their process information, and hence insight, without placing unreasonable demands upon their time. STADIUM-SOI enables process and device engineers to use simulation software immediately (without the typically steep learning curve) as well as include in their designs the effects of manufacturing variation on product yield.

Because time is so valuable, it is often the biggest obstacle one faces with respect to statistical computer simulation. First, most commercial software is hard to use and requires hours of practice before one has confidence in the results. Next, the total number of experimental design options is overwhelming and demands a great deal of time be spent studying statistics. Finally, the time involved in setting up and controlling a multiple (e.g. 32 run) simulation experiment from the process to the device level, including correct structure and variable substitution, is prohibitive.

STADIUM-SOI provides a push-button windowing environment that eliminates the need to memorize complicated and often cryptic simulator syntax. Default process step models are chosen specifically for SOI technology to optimize the accuracy of the simulations. Furthermore, statistical options are reduced to a complete set of default experiments. By following the logical progression of STADIUM's statistical design package, the engineer is led to a model of the response, estimated mean, estimated standard deviation, and factor contributions. The resulting statistical model is based on a response variable (e.g. Threshold Voltage) which is comprised of statistically derived coefficients multiplied by the process step variations (e.g. Channel Doping).

In regard to the statistical model, it has been argued that the estimated mean of a simulation output is strongly dependent upon proper tuning of the simulator to the process flow. Regardless of tuning, the estimated standard deviation of the output response and input factor contributions to that output can still provide valuable information on process trends. Therefore, process and device simulation and its use in the design of high yield ICs can be greatly enhanced through the use of statistics. Indeed, as simulation models improve, DoE methodology will become all the more effective.

The STADIUM-SOI main menu (Figure 3-1) invokes four modules, Process Design, Simulation Control, Simulation Output, and Statistical Analysis. The relationship between these modules is shown in the block diagram in Figure 3-2.

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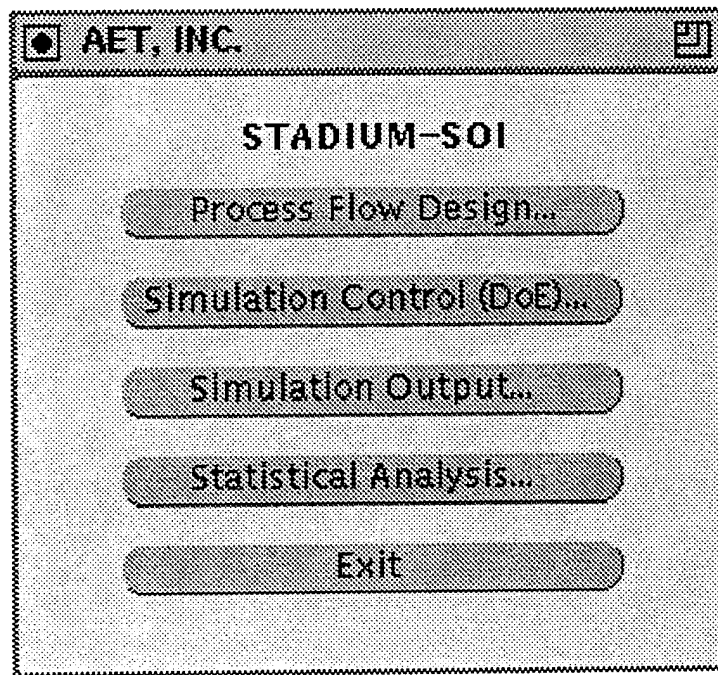
Figure 3-1: Main Menu
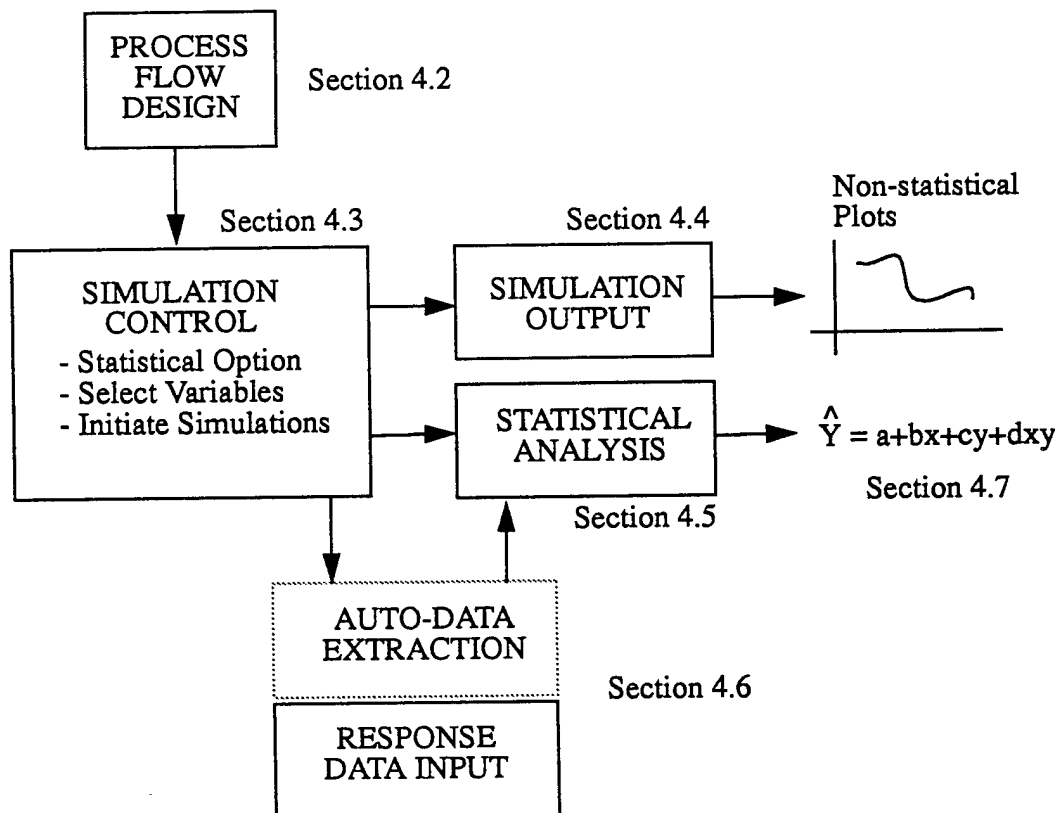
Figure 3-2: STADIUM-SOI Overview Diagram

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First, the Process Design module provides an easy-to-use interface designed to allow direct graphical creation of the process flow. The user need not look up, learn, or memorize any of the simulator-specific syntax. Process steps are selected (e.g. a button marked "Diffusion" is pushed) and the flow is automatically built with the correct syntax. This minimizes the chance of error and subsequent computer crashes. Next, many of the decisions (e.g., model selection) that confront the inexperienced user are preset through the use of default values. Default decisions are made from careful examination of simulations of typical SOI device structures and the combined contributions from experienced users (semi-expert system). This includes the grid design. The user may simply allow STADIUM-SOI to generate a grid structure that is appropriate for statistical simulation. Then, the Simulation Control module (Figure 3-3) is used as the simulation experiment "desktop" with the following built-in statistical capabilities:

- Nominal Simulation

- Sensitivity Analysis

- Screening (Plackett-Burman)

- Fractional Factorial Designs

- Full Factorial Designs

Figure 3-3: Simulation Control Menu

A nominal simulation is a single-run experiment with no input variation added. This single simulation run is used to determine if the device is valid. Next, variables are entered by selecting them (in a point & click fashion) in the simulation input file, entering the deviation (e.g. 1, 2, or 3 standard deviations or upper range), and assigning a name. Once the variables are established for a particular process, the appropriate statistical experiment design is selected. The selection displays the required runs and the level of modeling obtained for each particular choice. All of the information regarding the resulting model is dynamically provided in a clear format. In this way, the engineer is prompted to choose the experiment, not from a sophisticated knowledge of statistics, but rather based on the fundamental trade-off of runs (simulation time) vs. accuracy (model fit). Either the statistical standard deviation or the delta (= maximum value - mean) may be entered for the deviation. Simulations are run and the resulting data is analyzed. If the model is later found to be inadequate (based on R-squared value), the next level of experiment is chosen and a new DoE is generated.

The Simulation Output module is used to extract and analyze non-statistical data for any previously run simulation (e.g., I-V plots, grid, contour structures, field lines, doping profiles, etc.).

The Statistical Analysis module is divided into two functions: extraction and regression analysis. Data extraction collates the data and presents it in a form that is suitable for rapid identification and interpretation. Response variables are extracted and regression analysis performed by the statistical analysis module. The response variables that are automatically extracted are:

- Gate Oxide Thickness
- Peak Channel Doping
- Peak Source/Drain Doping
- Channel Length
- Transconductance
- Subthreshold Slope
- Breakdown Voltage

The objective of this procedure is to obtain information about the effect of process variation on the device yield which is accomplished through statistical analysis. Linear regression techniques are used to derive a model for an output response, estimated mean, estimated standard deviation, and factor contributions. The model is an equation comprised of statistically derived coefficients multiplied by the process and/or device variables (as identified by the experimenter). An example of a statistical model from MIT's Lincoln Labs SOI NMOS process is shown below.

V_t = - 4.5 + (-8.53e-4)init_oxide_temp + (4.66e-4)gate_ox_temp + (2.02)poly_litho

+ (1.09e-2)cont_imp_drive_temp + (3.05)silicon_thickness

Estimated Mean = 0.51 V I Estimated Standard Deviation = 6.72e-2 V I Rsq = 0.977 (good fit)

4. STADIUM-SOI Software Description

4.1 Main Menu

The STADIUM main menu and a brief description of the function of each button are shown in Figure 4-1. An overview of the entire STADIUM flow diagram is shown in Figure 4-2. The four main sections of the main menu are divided by their functionality. The Process Design is described in Section 4.2, Simulation Control in Section 4.3, Simulation Output in Section 4.4, and Statistical Simulation in Section 4.5.

Create the process flow step-by-step and add it to a library to be used later in experiments.

Load a library flow file and perform experiments on it. Every aspect of the multiple statistical simulation will be controlled from this one window.

Characterize the device that results from each run (e.g. oxide thickness, IV curves, etc.). Parameters are extracted automatically at the click of a button.

Analyze the response variables through regression analysis. The statistical model (e.g for Vt) will be determined along with factor contributions, estimated mean and standard deviations. The R-squared will be also calculated to test the fit.
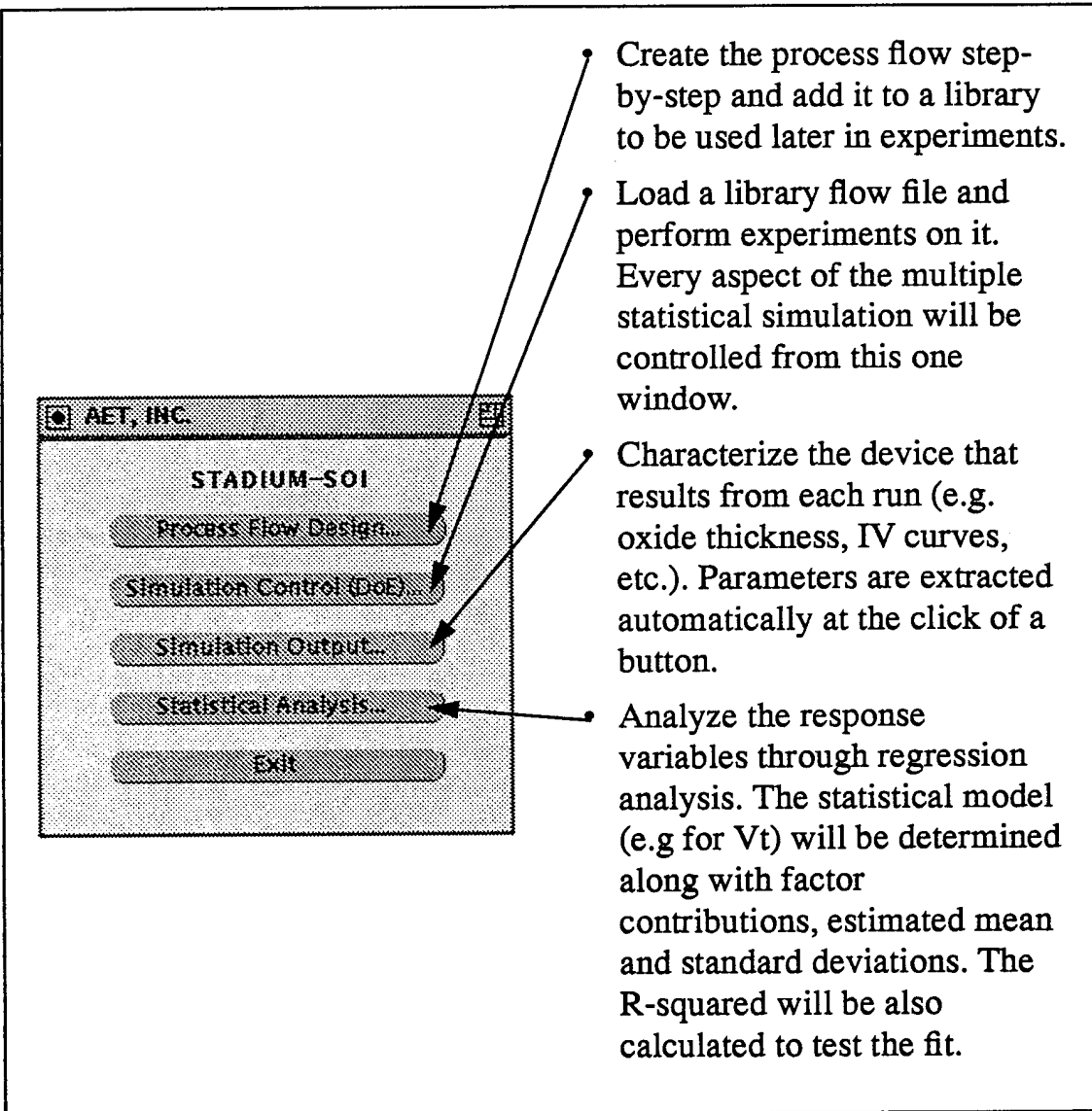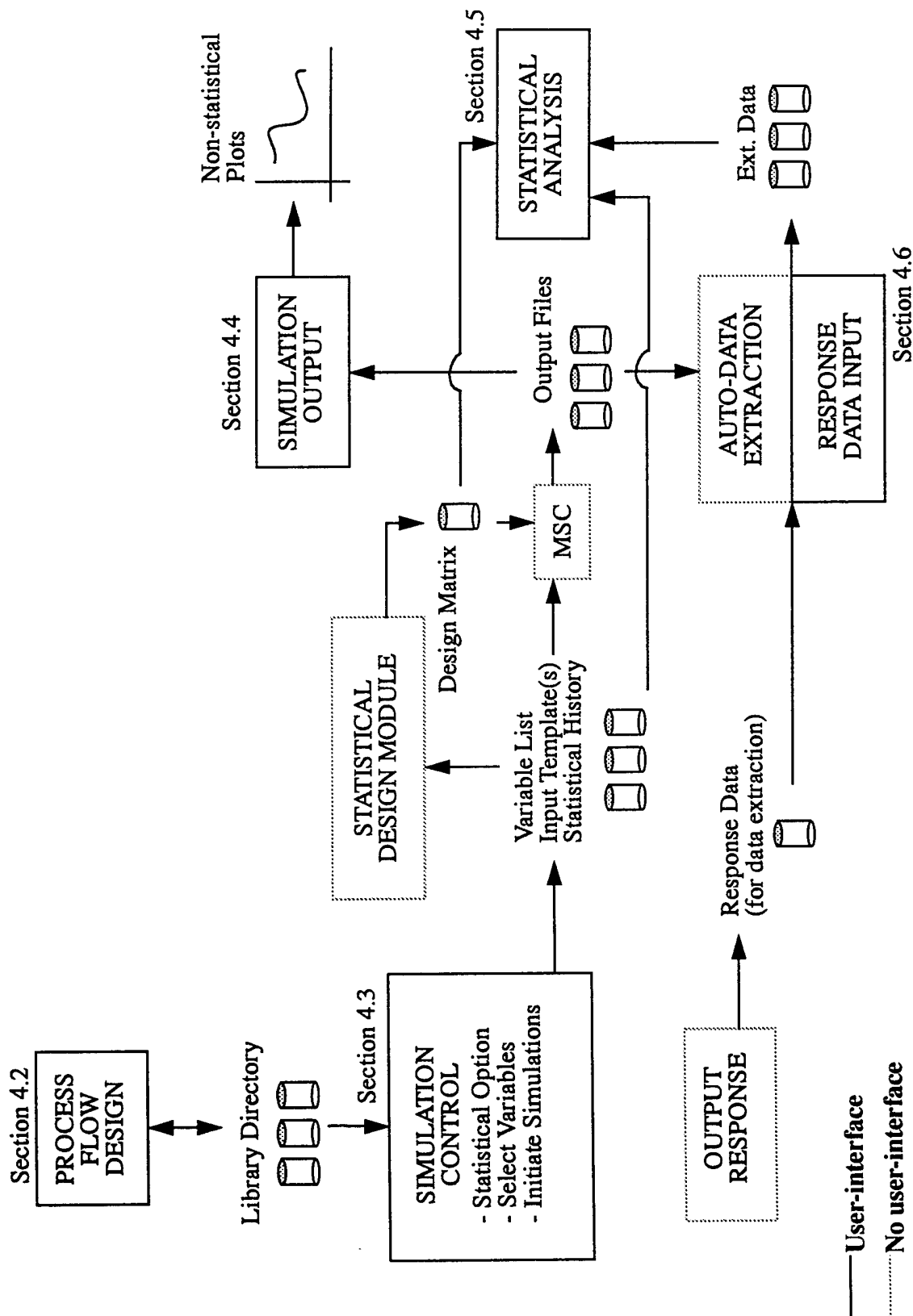
Figure 4-1: Main Menu

Figure 4-2: STADIUM-SOI Overview Diagram

4.2 Process Design

The process design window is used to build a process flow step-by-step and place it into a library file for use in statistical experiments. The creation of the process flow for simulation is greatly simplified through the use of push-button options (Figure 4-3).

Process steps in the flow are displayed (and can be edited) as they are constructed in the text window. Each of the buttons leads to a process-step-specific window (Figure 4-4). Once the step is entered, the window closes and the next step is chosen. No mistakes in syntax are possible through this method of entry, and all steps have built-in default values that minimize the required inputs.

Note, one is not limited to the choices shown in the window since additional parameters may be added to the step in the text window. Again, great efforts were made to minimize the selection to only those parameters typically known to process/device engineers. For example, an expert in process simulation may wish to tune the coefficients of the simulation diffusion equation to fit a particular flow (which is still possible). However, in STADIUM the novice is not confronted with this type of option in an attempt to simplify and expedite the process design procedure.
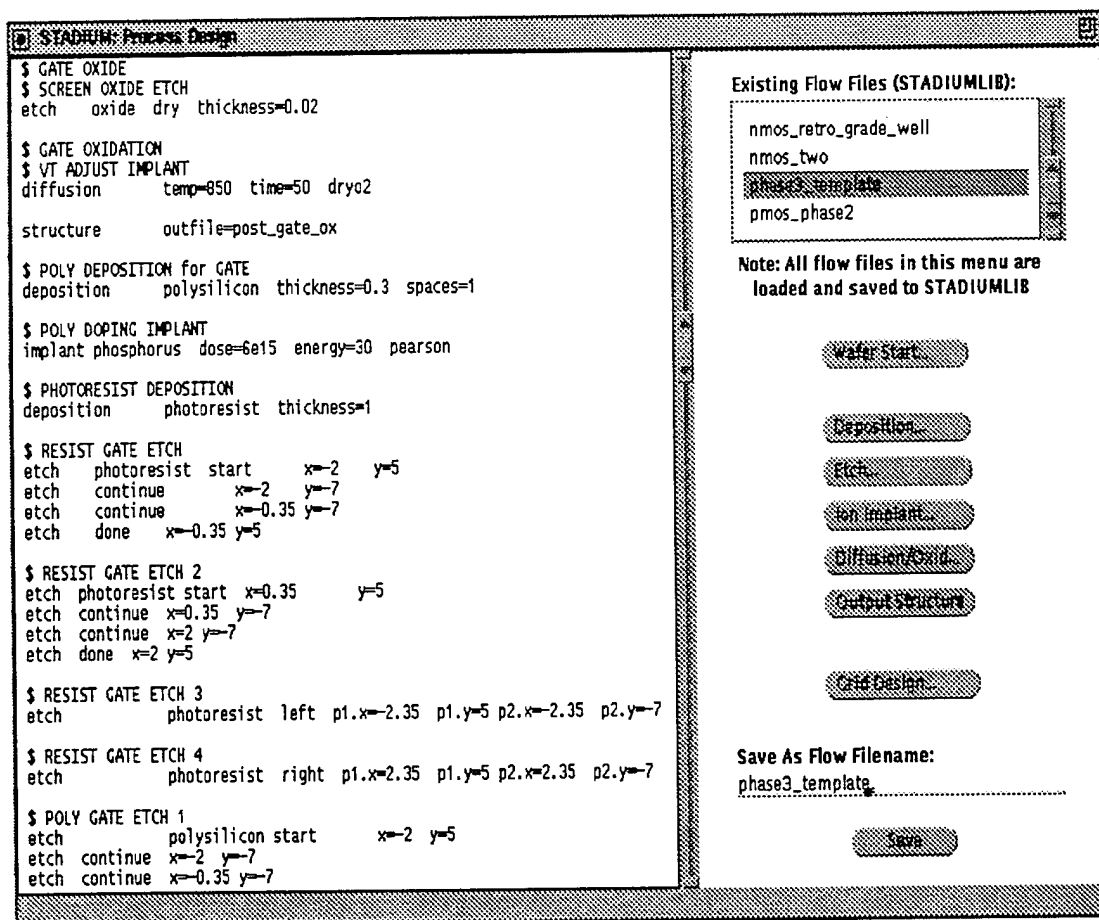

Figure 4-3: Process Design Top Menu

STADIUM|Process Design: Deposition

\<Deposition\>

Material: ▓ Silicon

Thickness (microns): ◆................

Impurity: ▓ Boron

Conc. (atoms/cm^3): _____ **Exp:** 15 ▲▼

Grid Divisions: 1 ___ ▲▼

▓▓▓ Include Heat Effect ▓▓▓

Time: ....

Temperature: _____

Comment: ....

(Write)

STADIUM|Process Design: Etch

\<Etch\>

Material: ▓ Silicon

Direction: ▓ Complex

Thickness: ....

1st Point	**X:**	**Y:** ....
2nd Point	**X:** _____	**Y:** _____
3rd Point	**X:** _____	**Y:** _____
4th Point	**X:**	**Y:** ....

Comment: ◆_____

(Write)

STADIUM|Process Design: Ion Implantation

\<Ion-Implantation\>

Impurity: ▓ Boron

Dose (atoms/cm^2): ◆_____ **Exp:** 15 ▲▼

Energy: _____

Tilt Angle (degrees): _____

Distribution: ▓ Dual Pearson

Comment: _____

(Write)

STADIUM|Process Design: Diffusion/Oxidation

\<Diffusion & Oxidation\>

Time (Minutes): ◆_____

Temperature (deg. C): _____

▓▓▓ Ramp the temperature ▓▓▓

End Temperature: _____

Ambient: ▓ Nitrogen

HCL (%): _____

Impurity: ▓ None

Conc. (atoms/cm^3): _____ **Exp:** 15 ▲▼

Comment: _____

(Write)

Figure 4-4: Process Design Sub Menus

The grid design menu is entered through the wafer start menu and is used to automatically generate a grid structure for the CMOS device (Figure 4-5). The grid is created in such a way as to maximize tracking of small variations in the device structure. This grid will be more dense than is typically used, but necessary to accurately model the statistical variation of the device. Four known device parameters are entered (A thru D) and the grid is instantly generated with the statements displayed in the Process Design text window. Automatic data extraction also uses this information to determine the appropriate points to extract data.

The user has two options to select from for the flow design: User Defined and Automatic. The automatic option provides a standard NMOS template for use as a beginning structure which one can use (or make modifications to) to design typical SOI CMOS devices. The user defined option simply generates the SOI wafer and corresponding grid.
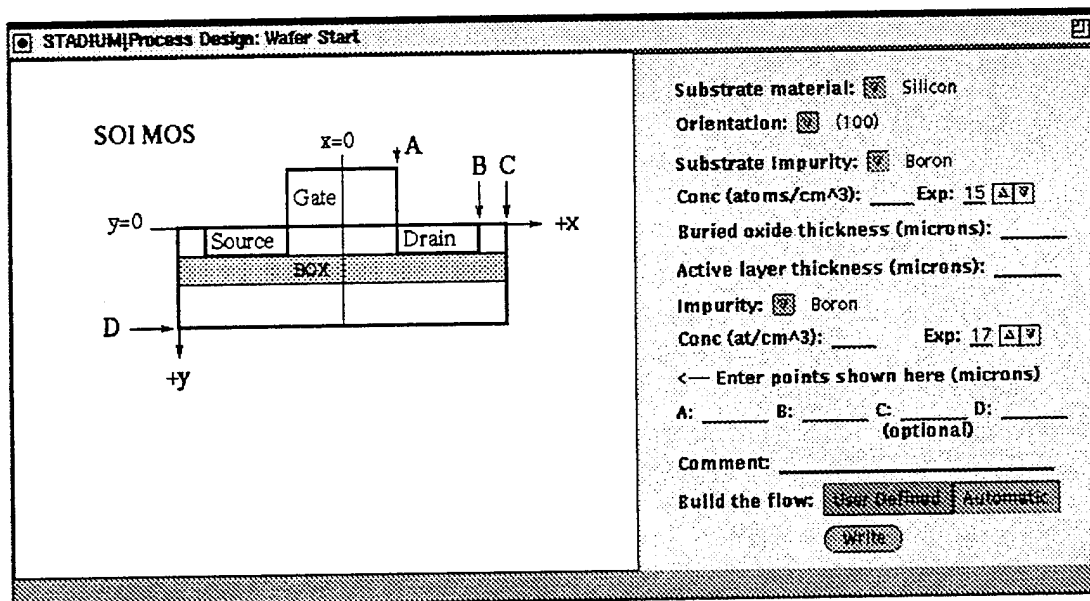

Figure 4-5: Wafer Start Menu

4.3 Simulation Control

The simulation control window is designed to be the simulation "desk top" on which statistical experiments are built, begun, and monitored (Figures 4-6 & 4-7). The following description provides an overview of the statistical simulation procedure and can be used to guide one through an experiment. For more complete coverage of statistical simulation refer to Section 4.7, STADIUM Statistical Methodology.

First, a file is selected and loaded from the library. This file becomes the simulation "template" that is used to perform a series of experiments (without affecting the original library file) and is displayed in the text (lower left) window. Library files can be process, device, or any other standard text-based input file (e.g., SPICE netlist). One library is set up for each simulator employed in the series, i.e. outputs from one are configured to feed into the next one and so on.

Then, a nominal experiment is selected. Nominal refers to an experiment with no input variation added (a typical non-STADIUM simulation). This single simulation run is used to determine if the template files are correct and the device is valid. Once the nominal simulation is complete, the data is accessed (e.g., gate oxide thickness, Vt, etc.) through the Simulation Output window (described in Section 4.4).

Next, variables are entered by pointing them out in the simulation input file, entering the deviation (e.g., 1, 2, or 3 standard deviations or upper range), and assigning a name. The variable and its corresponding information will then be displayed in the Variable List. Editing variables is accomplished by selecting them, changing the deviation, temporarily turning them off, or deleting them entirely.

Once the variables are established for a particular process, the appropriate statistical experiment design is selected. The selection shows the required runs and the level of modeling obtained for each particular choice. All of the information regarding the resulting model is provided dynamically in an clear format. In this way, the engineer is prompted to choose the experiment, not on a sophisticated knowledge of statistics, but rather, based on the fundamental trade-off of runs (simulation time) vs. accuracy (model fit). The statistical standard deviation or delta (maximum value - mean) may be entered for the deviation. A choice of 1, 2, or 3 sigma is available and is simply the deviation value correspondingly multiplied by 1, 2, or 3.

For the following refer to Figure 4-7, the full Simulation Control window. To complete the procedure, runfiles are built and the simulations are executed. The output for each simulation is displayed in the terminal (upper left) window while it is running. The resulting data is then analyzed in the Statistical Analysis window. If the model is later found to be inadequate (based on R-squared value), the next level of experiment is chosen and run in the same directory.

All files generated by STADIUM can be accessed and edited through the display option. This function allows oversight of the simulation experiment insuring proper execution and provides flexibility to the more experienced user.

Figure 4-6: Right Half of Simulation Control Menu

STADIUM: DoE Simulation Control

pram phelps 1: SIMULATION OUTPUT IS SHOWN HERE...

```
$ TMA TSUPREM4 NMOS transistor simulation

$ Define the grid
MESH      GRID.FAC=1.9
METHOD    ERR.FAC=2.0

$ Initialize the structure
INITIALIZE <100> BORON=5E14

$ Initial oxidation
DIFFUSION TIME=30 TEMP=1000 DRY HCL=5

$ Nitride deposition and field region mask
DEPOSIT   NITRIDE     THICKNESS=0.07 SPACES=4
DEPOSIT   PHOTORESIST POSITIVE THICKNESS=1
EXPOSE    MASK=field
DEVELOP
ETCH      NITRIDE     TRAP
ETCH      OXIDE       TRAP UNDERCUT=0.1
ETCH      SILICON     TRAP THICKNES=0.25 UNDERCUT=0.1

$ Boron field implant
IMPLANT   BORON DOSE=5E12 ENERGY=50 TILT=7 ROTATION=30
ETCH      PHOTORESIST ALL

$ Field oxidation
METHOD    PD.TRANS    COMPRESS
DIFFUSION TIME=20     TEMP=800   T.FINAL=1000
DIFFUSION TIME=180    TEMP=1000  WET02
DIFFUSION TIME=20     TEMP=1000  T.FINAL=800
ETCH      NITRIDE     ALL

$ Unmasked enhancement implant
```

Current Simulator #: 1 [4]▼ TSUPREM4

tmp_trench

# of Runs   4   8   16   32   64   128

Normal | Scanning | Full factorial | Fractional

4 Variables -> Statistical Resolution IV
Main Effects with 2 variable interactions

Total Activated Variables for All Simulators: 4

Create a Variable   Name: VAR5

Deviation from mean value: 1

Put the POINTER directly in FRONT of the variable
value in the simulation input file and press add.

e.g. TIME = ^1000   Add

Variable List   Activated: 4   Subtotal: 4

[initial oxidation temp] 30   +/-   2   ION
[nitride thickness]   0.07 +/-   0.01 ION
[oxide undercut]   0.1   +/-   0.01 ION
[final temp fox]   1000 +/-   1   ION

1 sigma   ON/OFF | Delete

Display:
Simulation Run File(s)
1 ___ [4]▼ Out of: 8 ___

Save Changes
Build Run File
Start Simulations

Figure 4-7: Simulation Control Menu

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4.4 Simulation Output

The simulation output is used to extract and analyze non-statistical data for any previously run simulation (Figure 4-8). This module considers one device structure or I-V runfile at a time. Information regarding one dimensional and two dimensional slices is provided. I -V plots are also available for structures run through the device level. Print statements display data in the text window and plots are shown in separate windows.
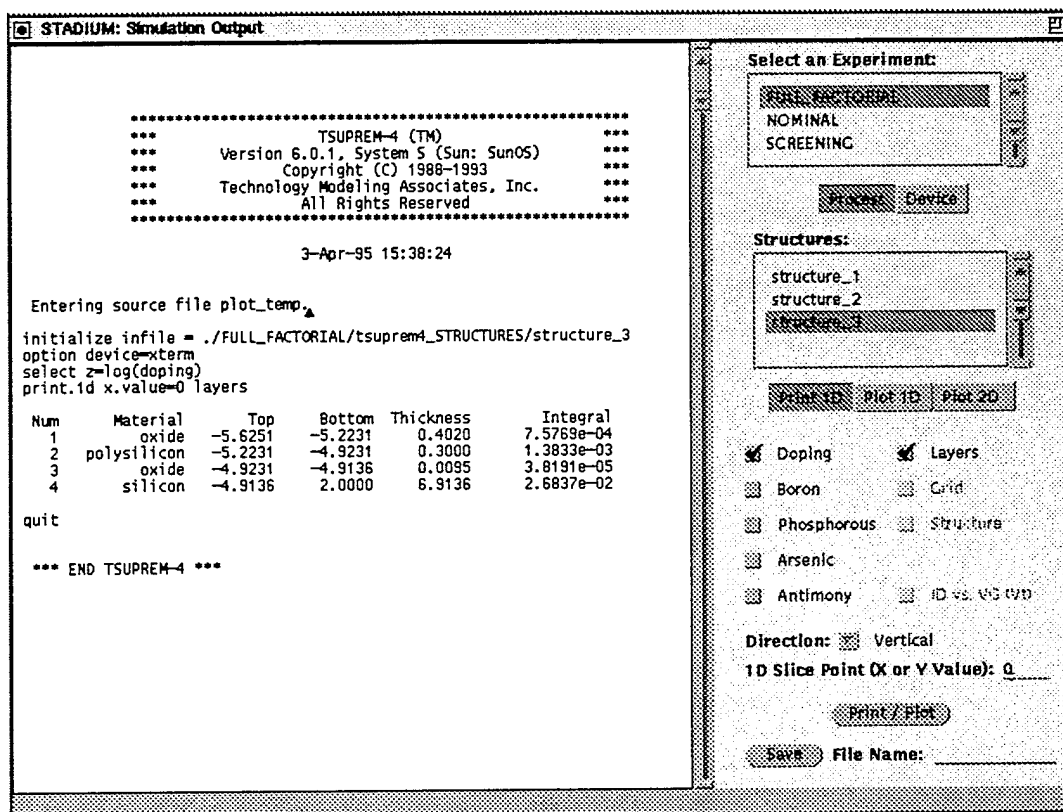

Figure 4-8: Simulation Output Menu

4.5 Statistical Analysis

The statistical analysis derives a statistical model for an output response, estimated mean, estimated standard deviation, and factor contributions. Response data refers to any output value that the simulator provides that is of interest to the experimenter. The model is an equation comprised of statistically derived coefficients multiplied by the process and/or device variations (as identified by the experimenter).

The statistical analysis top menu provides two main functions: first extract and then perform regression analysis on the response data (Figure 4-9). Several parameters known to be important to MOS devices are automatically extracted. However, it is possible that some factors exist which have not been automatically extracted or one may wish to view the response data previously extracted. For this reason, selecting the Response button provides an easy-to-use hand data extraction window (Section 4.5.2). Selecting an output response from the list of possible choices

invokes the regression analysis routine and data pertaining to factor contributions (in the case of screening) or model information is displayed in the text window.Finally, the Print Data button sends the text file to the configured printer. For more information regarding the regression analysis, refer to Section 4.8.1.

STADIUM: Statistical Analysis

Select an Experiment for Analysis

FULL FACTORIAL
NCH
NOMINAL

OUTPUT RESPONSE DATA EXTRACTION

- gate oxide thickness
- channel surface charge
- effective channel length
- source/drain junction depths
- source/drain peak doping
- threshold voltage
- transconductance
- subthreshold slope
- breakdown voltage

Process   Device   Response

Percent of Extraction Complete:

<add or edit a response>

Output Response Variable

effective_channel_length
sub_threshold_voltage
threshold_voltage

Print Data

Full Factorial Analysis

$Y = -4.503683 + (-0.000853338)temp1 + (0.00466515)VAR10 + (2.01955)VAR15 + (0.00108795)VAR26 + (3.05125)silicon\ thickness$

Rsq = 0.977049
Estimated Mean = 0.514420
Estimated Standard Deviation = 0.067179
Factor Contributions:
temp1 : 1.58 %
VAR10 : 56.25 %
VAR15 : 3.53 %
VAR26 : 3.78 %
silicon thickness : 34.86 %

Figure 4-9: Statistical Analysis

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4.5.1 STADIUM's Systematic Approach

By following a systematic approach, it is possible to gain valuable process insight with a minimum number of simulation runs. This systematic approach is illustrated in Figure 4-10 and is then described in detail in Section 4.7. As stated earlier, the experimenter or researcher need not get caught up in the statistical theory. That is automatically done by STADIUM. A basic understanding of this approach and what is obtained at each stage is all that is required to perform sometimes complex statistical experiments.
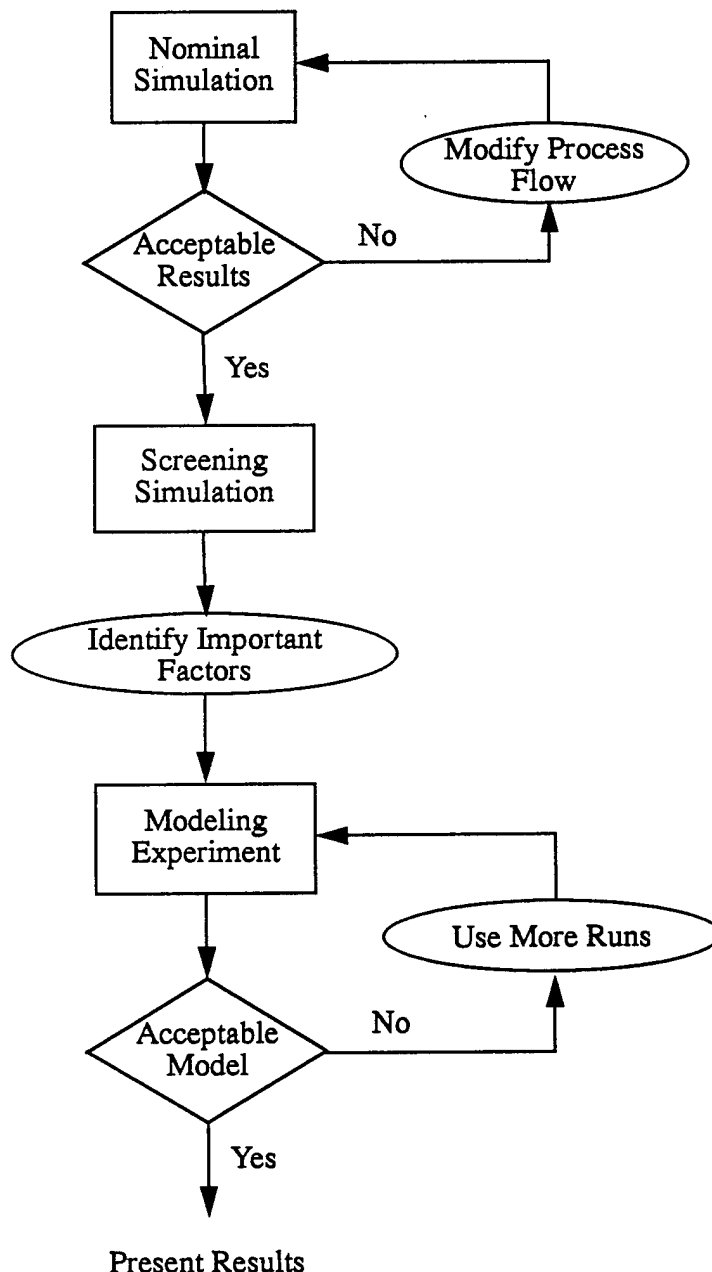

Figure 4-10: Illustration of STADIUM's Statistical Methodology

4.5.2 Response Data Menu

The response data menu is used to edit or the add response variables. If a response variable is selected when the Response button is pushed, all data pertaining to this variable will be loaded into the response data menu. The data can be compared to the output file that it was derived from and edited if changes are needed (e.g., disagreement with STADIUM's interpretation of effective channel length).

One may wish to analyze a piece of output data that has not been extracted. If no response variable is selected prior to pushing the response button, the first in the series of output files (e.g., 1 of 16) is automatically loaded. The desired item is selected from the output file and added to the data value table. After add is selected, the value is entered in the data value table, the next file is loaded, and so on (e.g.,16 times). The value in the table always corresponds to the output file that is currently loaded, i.e. it is impossible to enter the wrong value because output file 3's data cannot be entered into table value position 2. Also, to simplify the procedure in long output files, once the position of the desired data in the first file is selected, the next file is loaded referencing the same location. Once all values are entered, the response is assigned a name and saved. The new response will then be displayed in the response variable list and selecting it will display the statistical regression information in the text window.

4.6 Automatic Data Extraction

STADIUM has the capability to extract selected process and device parameters. For the automatic data extraction to work correctly, the STADIUM automatic gridding program must be used to "lay out" the device structure. This ensures that STADIUM knows where the important regions of the device are located. The automatic data extraction may be used for any type of experiment; nominal, screening, full or fractional factorial experiments. How each parameter is extracted will now be discussed in detail. The data that is automatically extracted is listed below.

- Gate Oxide Thickness
- Channel Peak Doping
- Source/Drain Peak Doping
- Channel Length
- Transconductance
- Subthreshold Slope
- Breakdown Voltage

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4.6.1 Oxide Thickness and Channel Surface Charge

STADIUM "cuts" the structure vertically directly under the center of the gate when extracting oxide thickness and channel surface charge. This is shown for a hypothetical device in Figure 4-11.
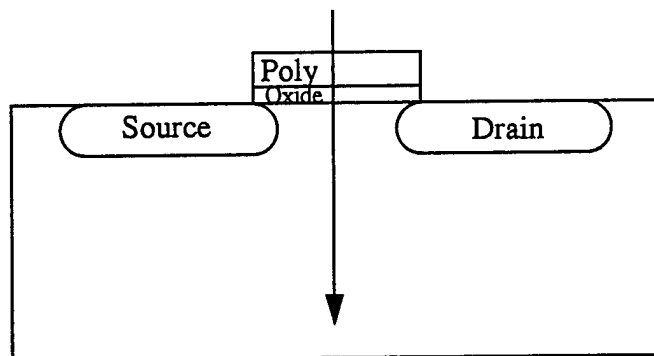

Figure 4-11: Illustration of Oxide Thickness and Channel Surface

The gate oxide thickness is determined to be the thickness of the oxide layer directly above the silicon. The gate contact material is unimportant and may be polysilicon, aluminum, or no material at all. The channel surface charge is determined to be the charge at the first grid point in silicon directly under the gate.

4.6.2 Source / Drain Junction Depth and Peak Doping

When extracting the source / drain junction depths and peak doping, STADIUM "cuts" the structure vertically through the center of the drain region. This is shown for a hypothetical device in Figure 4-12.
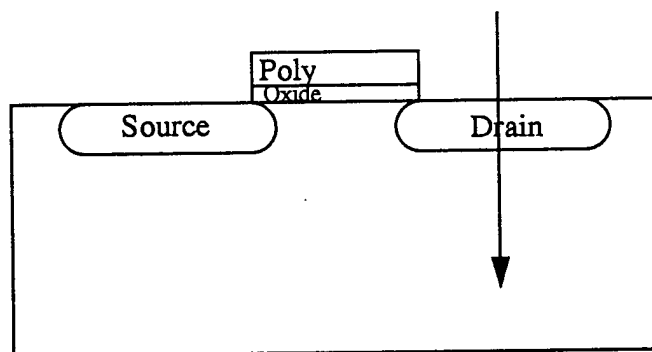

Figure 4-12: Illustration of Junction Depth and Peak Doping Extraction

The top of the drain region is defined as the coordinate of the first grid point in the silicon and the bottom of the drain region is defined as the coordinate of the first grid point in the Silicon where the doping type changes. The difference in these two coordinates is the junction depth. The doping is checked at each grid point in the drain region and the highest value of doping in that region is the peak doping.

4.6.3 Effective Channel Length

The effective channel length is determined by the amount of lateral diffusion of the source and drain under the gate. To remain consistent over each simulation, the effective channel length is extracted at half of the source / drain junction depth. This is shown in Figure 4-13.
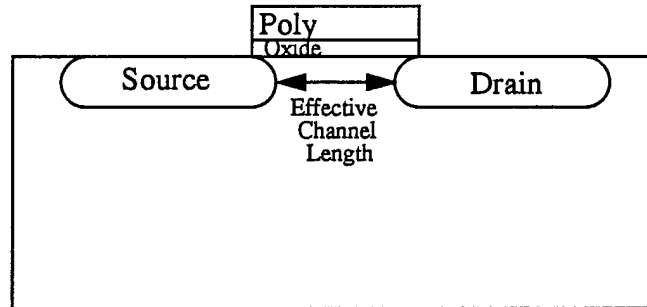

Figure 4-13: Illustration of Effective Channel Length

4.6.4 Threshold Voltage and Maximum g_m

Threshold voltage and the maximum transconductance are the two device level parameters that STADIUM automatically extracts. MEDICI produces a plot of collector current vs. gate voltage as shown in Figure 4-14.
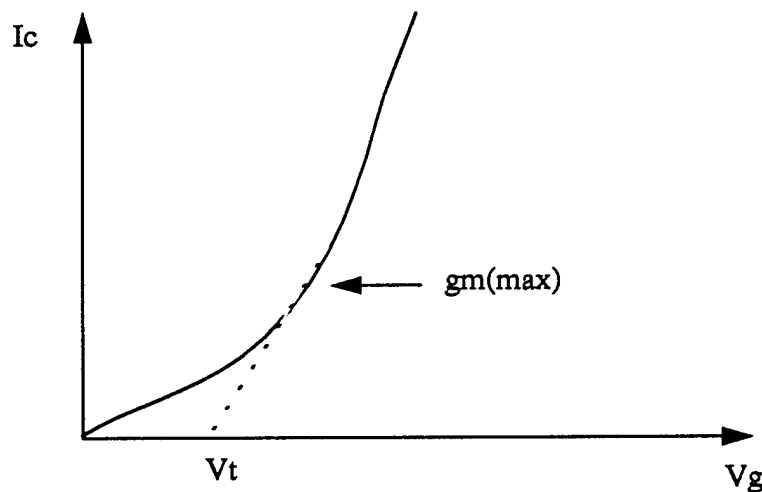

Figure 4-14: Illustration of Threshold Voltage and Transconductance

The threshold voltage is determined by first finding the point on the curve where the maximum slope occurs. Points on either side of this point of maximum slope are used to extrapolate a line to the Vg axis. This intercept is defined as the threshold voltage. Simply, the maximum slope of the curve is defined as the maximum gm.

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4.6.5 Subthreshold Slope

Subthreshold Slope is a device level parameter that STADIUM automatically extracts. MEDICI produces a plot of collector current vs. gate voltage as shown in Figure 4-15.
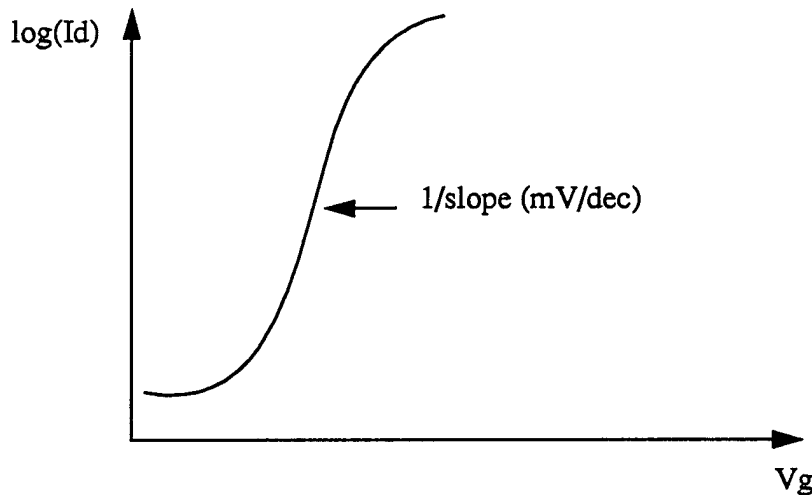

Figure 4-15: Illustration of Subthreshold Slope

The subthreshold slope is determined by first finding the point on the curve where the maximum slope occurs. The inverse of this is used as the subthreshold slope.

4.6.6 Breakdown Voltage

Breakdown voltage is a device level parameter that STADIUM automatically extracts. MEDICI produces a plot of collector current vs. drain voltage as shown in Figure 4-16.
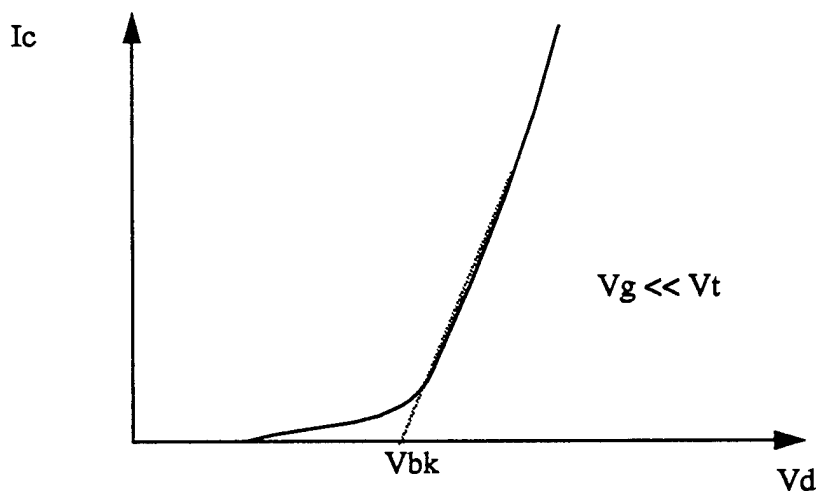

Figure 4-16: Illustration of Subthreshold Slope

The breakdown voltage is determined by first finding the point on the curve where the maximum slope occurs. Points on either side of this point of maximum slope are used to extrapolate a line to the Vd axis. This intercept is defined as the breakdown voltage.

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4.7 STADIUM Statistical Methodology

STADIUM is designed for easy selection of various statistical experiments. Because of STADIUM's built-in design matrix generator and intelligent software, very little knowledge of statistics or design of experiments is required to achieve powerful results. The statistical analysis is performed within STADIUM with the emphases on the result and not statistics. This section is provided only as a reference to those users who wish to know more about STADIUM's statistical methodology.

4.7.1 What is a Statistical Experiment?

A statistical experiment (often called an experimental design or design of experiment) consists of purposeful changes of the inputs (factors or variables) of a process in order to observe the corresponding changes in the outputs (responses). Thus, a statistical experiment is a scientific approach which allows the researcher to better understand a process and to determine how the inputs affect the response. An illustration of a process is shown in Figure 4-17.
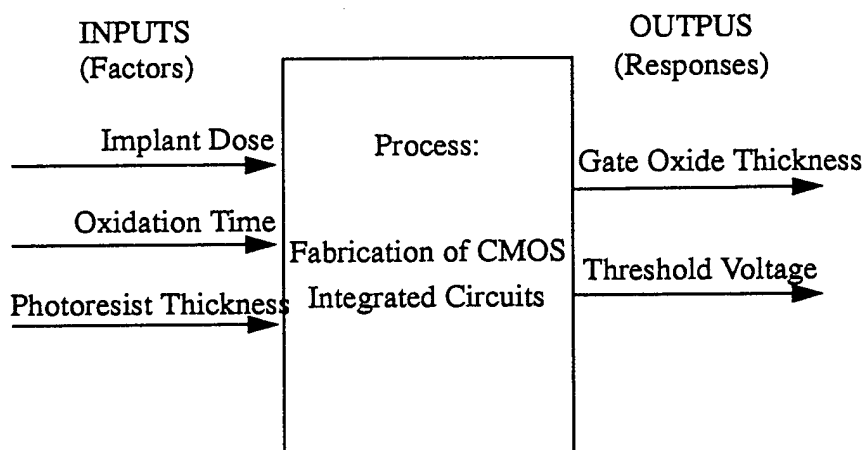

Figure 4-17: Illustration of a Process

One-factor-at-a-time experimentation or Monte Carlo methods, because of their simplicity, have often been used to predict the impact of factor variation on a response. These methods suffer from a number of related difficulties. A large number of simulation runs are needed to obtain an accurate estimate and the estimate does not provide any information such as how the response varies as a function of input factors. These methods can no longer be tolerated if a company intends to keep up in a highly competitive market.

A carefully planned approach for conducting a statistical experiment, however, can give valid insight regarding how each factor affects the response. This statistical design of experiment methodology has been used successfully in manufacturing process development for many years. It involves complex statistics and is often fully understood only by statisticians. STADIUM takes care of the statistics internally and presents an easy-to-understand methodology for performing a statistical experiment.

4.7.2 Nominal Simulation

The first step in STADIUM's systematic approach is the Nominal Simulation. As the name implies, all the input variables are set at their nominal, or mean value. STADIUM then performs a single simulation with the variables set at their nominal values. The purpose of the Nominal Simulation is to check the process. If an error has been made in the process, it is much better to catch it after one simulation rather than eight or sixteen.

The Nominal Simulation may also be used to "tune" the simulator. Many simulation "gurus" force the simulator to match experimental data by modifying such parameters as diffusion coefficients and carrier lifetimes. Since the STADIUM methodology is more concerned with predicting trends, this practice is usually unnecessary. The Nominal Simulation should be thought of as more of a "sanity check" of the process.

4.7.3 Screening Experiment

Once the process has been successfully simulated with the factors set at their nominal levels, a Screening Experiment is performed. The purpose of screening is to reduce a large number of factors to a smaller set of important factors for subsequent experimentation. STADIUM uses Plackett-Burman designs for its screening experiments. Plackett-Burman designs are based on Hadamard matrices where the number of runs in Hadamared matrix is a multiple of 4 (as opposed to powers of 2 for conventional designs). Designs of this type are advantageous not only for their lower number of runs but for their confounding patterns. In non-geometric Plackett-Burman designs (which are used in STADIUM) each two-factor interaction is partially confounded with each of the factors. This provides the best measure of each factor's effect on the response in the least possible number of runs. The number of runs in a Plackett-Burman design are based on the number of factors. Table 4-1 describes the Plackett-Burman screening designs used in STADIUM.

Table 4-1: Plackett-Burman Screening Designs

FACTORS	RUNS
8 - 11	12
12 - 19	20
20 - 23	24
24 - 27	28
28 - 35	36

The purpose of screening is to identify those factors that affect the response. It has been found that factors which contribute more than 5% to the variance of the response should be considered "important" and those which contribute less than 5% may be "discarded" as "unimportant". It is not uncommon to perform a screening experiment with over 30 factors and find less than 10 factors important.

4.7.4 Modeling Experiment

The next step in the STADIUM systematic approach is the modeling experiment. The goal of the modeling experiment is to mathematically relate the response to the input factors in the form of an equation. This equation is called a "model". This model allows the estimation of the response at

levels other than those used in the experiment. It is from this model that STADIUM calculates an estimated mean and variance for the response.

The simplest form of a statistical model for 3 factors is given in Equation 4.1.

$$\hat{Y} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_3 X_3 \qquad \text{(Eq. 4.1)}$$

where the β's are coefficients determined by STADIUM and the X's are the factors. This equation relates the response, Y, to each of the factors. The symbol Y "hat" denotes that the response is "estimated". A more complex equation may be obtained by including "interaction terms". An equation of this type for 3 factors is shown in Equation 4.2.

$$\hat{Y} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_3 X_3 + \beta_{12} X_1 X_2 + \beta_{13} X_1 X_3 + \beta_{23} X_2 X_3 + \beta_{123} X_1 X_2 X_3 \quad \text{(Eq.4.2)}$$

Different modeling experiments yield different types of modeling equations and STADIUM automatically generates the appropriate modeling equation for each experiment. The two types of modeling experiments used in STADIUM will next be presented.

1. Full Factorial Experiment

The number of simulation runs for a full factorial design of k factors is 2^k. For example, a full factorial design for 3 factors requires 2^3 or 8 runs. One advantage of a full factorial experiment is the ability to produce a model that contains all possible interaction terms. The obvious disadvantage is the simulation time required to perform the experiment. Full factorial experiments become "expensive" quickly with 16 runs required for 4 factors, 32 runs required for 5 factors, 64 runs required for 6 factors, and 128 runs required for 7 factors.

2. Fractional Factorial Experiment

With the sometimes lengthy simulation times encountered in process and device simulation, full factorial designs are not often feasible. By not running a full factorial design, the ability to include all interactions in the model is lost, but seldom are interactions other than two-factor interactions very important.

A type of design that allows all factors and some interactions in the model while at the same time requiring fewer runs is a fractional factorial design. As the name implies, a fractional factorial design is a fraction or subset of a full factorial design. The generation of these designs is often complicated and tedious, as there are many different fractional factorial designs possible for the same number of factors.

Instead of presenting the fractional factorial designs in terms of often confusing statistical vocabulary such as "resolution", "confounding", and "aliasing", STADIUM simply presents the selection in terms of the number of runs and takes care of the statistics internally. If a fractional factorial design does not exist for a particular number of runs, STADIUM displays a warning message.

A potential disadvantage in using fractional factorial designs is the "quality" of the model, or how accurately the model predicts the data. A general rule of thumb (and trade-off) is that experiments with a higher number of runs produce "better" models. A more detailed discussion on the quality

of the model is presented in Section 4.8.4.

For the "statistically inclined", the types of fractional factorial designs offered in STADIUM are shown in Table 4.7.4-1.

Fractional Factorial Designs in STADIUM

Runs	3	4	5	6	7	8	9	10
4	Res III							
8		Res IV	Res III	Res III	Res III			
16			Res V	Res IV	Res IV	Res IV	Res III	Res III
32				Res VI	Res IV	Res IV	Res IV	Res IV
64					Res VII	Res V	Res IV	Res IV
128						Res VIII	Res V	Res V

4.8   STADIUM's Statistical Analysis

STADIUM automatically performs a statistical analysis for each response. This analysis results in the creation of the statistical models. These models are then used to calculate other important statistical quantities.

4.8.1   Regression Analysis

To obtain models of the form shown in Equation 4.1, STADIUM perform a classical regression analysis on the data. The model shown in Equation 4.1 can be represented in an equivalent matrix form as shown below.

$$Y = X\bar{\beta} \qquad\qquad \text{(Eq. 4.3)}$$

where

$$Y = \begin{bmatrix} y_1 \\ y_2 \\ y_3 \end{bmatrix} \qquad\qquad \text{(Eq. 4.4)}$$

$$X = \begin{bmatrix} 1 & X_{11} & X_{12} & X_{13} \\ 1 & X_{21} & X_{22} & X_{23} \\ 1 & X_{31} & X_{32} & X_{33} \end{bmatrix} \qquad\qquad \text{(Eq. 4.5)}$$

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and

$$\bar{\beta} = \begin{bmatrix} \beta_0 \\ \beta_1 \\ \beta_2 \\ \beta_3 \end{bmatrix} \qquad \text{(Eq. 4.6)}$$

To determine beta such that

$$Y = X\bar{\beta} \qquad \text{(Eq. 4.7)}$$

STADIUM solves the following least squares regression equation.

$$\bar{\beta} = (X'X)^{-1}X'Y \qquad \text{(Eq. 4.8)}$$

to produce a regression model equation of the form shown in Equation 4.1. A more generic form of Equation 4.1 for n factors is shown in Equation 4.9.

$$\hat{Y} = \beta_0 + \sum_{i=1}^{n} \beta_i X_i \qquad \text{(Eq. 4.9)}$$

4.8.2   Estimated Mean and Variance

STADIUM uses Equation 4.9 to estimate the response's mean. The mean values of each factor, $\bar{X}_i$, are substituted for the X_i's and Equation 4.10 is solved to produce the estimated mean. This estimated mean is displayed in STADIUM's Statistical Analysis window.

$$\hat{Y} = \beta_0 + \sum_{i=1}^{n} \beta_i \bar{X}_i \qquad \text{(Eq. 4.10)}$$

An estimate of the response's variance is obtained by using a first order Taylor expansion shown in Equation 4.11.

$$Var(Y) = \sum_{i=1}^{n} \left(\frac{d}{dX_i}\hat{Y}\right)^2 Var(X_i) \qquad \text{(Eq. 4.11)}$$

For the linear model in Equation 4.9, the first order Taylor expansion yields the expression for the estimated variance of the response, Y, shown in Equation 4.12. The variance of each factor,

$$Var(Y) = \sum_{i=1}^{n} \beta_i^2 Var(X_i) \qquad \text{(Eq. 4.12)}$$

$Var(X_i)$, is known from when the factor was added to the experiment in the Simulation Control window.

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4.8.3 Factor Contributions

In addition to the statistical model, estimated mean, and estimated variance, STADIUM calculated each factors contribution to the variance of the response. These factor contributions are used in screening to determine which factors are "important" in affecting the variability of the response. STADIUM calculates the contribution of factor X_i as shown in Equation 4.13.

$$\text{Contribution of} X_i = \frac{\beta_i^2 Var(X_i)}{\sum_{j=1}^{n} \beta_j^2 Var(X_j)} \qquad \text{(Eq. 4.13)}$$

4.8.4 Model Fit

STADIUM gives an indication of how well the model predicts the data. This can also be thought of as how good or bad the model and the data agree or "fit". STADIUM calculates the quantity shown in Equation 4.14.

$$R^2 = \frac{\sum_{i=1}^{n} (\hat{Y}_j - \bar{Y})^2}{\sum_{i=1}^{n} (Y_j - \bar{Y})^2} \qquad \text{(Eq. 4.14)}$$

R^2 is often referred to as the proportion of the variability in the data that is accounted for by the model. Clearly, the closer R^2 is to 1, the more response variation is accounted for and the model may be viewed as accurate.

5. Statistical Circuit Simulation

5.1 Introduction

The development of statistical circuit simulation techniques has led to the creation of a prototype software package known as STADIUM CKT. STADIUM CKT like all other STADIUM products utilizes design of experiments (DoE) to produce statistical models and insight into a particular technology. In this case that technology is circuit simulation. STADIUM CKT is the first version of a MS Windows based program which drives the circuit simulator PSpice in a statistical mode. As with all other STADIUM products this involves 4 basic steps, input specification, statistical simulations, output data extraction, and statistical analysis. The general goal of STADIUM CKT is to make this statistical circuit simulation process as easy as possible to use, giving this power to even the statistics novice. This is accomplished through a menu system which presents choices and information in a straightforward and intuitive manner. The main menu through which all of STADIUM CKT's power is reached can be seen in figure 5-1. The 4 steps of the simulation process will now be explained, emphasizing the ease of use of the STADIUM CKT methodology.
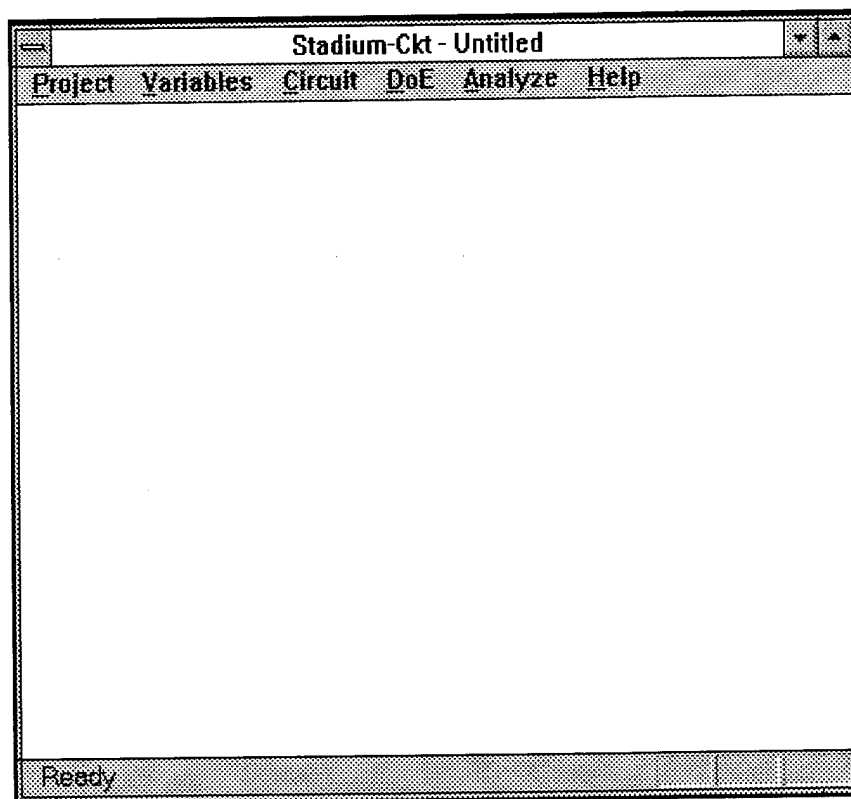

Figure 5-1 Main Menu

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5.2 Input Specification

The specification of inputs involves three main steps. These are creation of a netlist file, identification and specification of statistical component parameters, identification and specification of statistical model parameters, and correlation of these input factors. The netlist file can be generated by hand or through the use of a schematic capture program. After creation, this file is given to STADIUM CKT which analyzes it and creates internal tables representing all possible component and model variables. These internal tables are then used in the specification of component variables. The user is presented with a dialog box such as that seen in figure 5-2, which is used to specify the component variables.

Figure 5-2 Component Variable Specification

Each component supported by STADIUM CKT is listed from the netlist file in the Components list. The parameters associated with a component selected in this scrolling list are listed in the Parameters list to the right. Likewise, when a parameter is selected in the parameter list, statistical data is shown in the text fields above these two scrolling lists. Assigning a sigma value to a variable will cause it to be included in the list of variables submitted to the design of experiments module. When you click on Save Component with the mouse, all changes to the selected component are saved.

The specification of model parameters is done in a manner very similar to the specification of component parameters. The dialog box which is used is almost identical to that used for components, again making the job of learning STADIUM CKT very easy.

The final step in the input specification process is the correlation of the input variables presented above. In addition to parameter distributions, statistical modeling of circuit responses must also take into account circuit input parameter correlations within a device and between devices. SPICE models take care of most correlations within a device. However, STADIUM CKT also allows correlations to be specified between devices. These correlations are important because parameter matching of resistor ratios, transistor

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V_{BE}, IS, and Beta differences are critical design parameters in analog IC applications (e.g., current sources and differential amplifiers where identical supply currents and offset voltages are desired).

The methodology developed here, to support correlation between devices is a practical approach where design of experiment factorial designs involve discrete high and low factor levels. Thus, correlation values of -1 and +1 are the only values that can be assigned between circuit parameters. A correlation of "-1" indicates that the parameters are totally (or highly) inversely correlated. The opposite is true of a correlation of "+1" which implies that the parameters are totally (or highly) directly correlated to one another. This is the way in which STADIUM CKT tracks parameter correlations between devices and within a device that are assigned by the person using STADIUM CKT model and component specifications.

Figure 5-3 Correlation Specification

To set the Correlation parameter variables select **Correlation.** As seen in Figure 5-3, the variables list includes all variables for the current project. For example, three variables and one independent variable could have a correlation of "+1". The variable VAF, if selected, could be correlated to Beta by also selecting Beta in the independent variable list. VAF could be given a negative correlation to Beta by choosing "-1" in the correlation box. To complete the correlation, click on **Save** in the menu.

5.3 Statistical Simulation

The statistical simulation involves the selection by the user of a specific type of designed experiment which STADIUM CKT uses to generate the various netlists as well as to execute the multiple PSpice simulations. There are in general two types of experiments, screening designs and designs for manufacturing. Screening designs are used to determine the most significant input factors, while designs for manufacturing are used to develop statistical models for a particular circuit.

Screening designs in STADIUM CKT are specified automatically with the click of a button. STADIUM CKT takes the number of variables which are present and from this determines the proper type of screening design. No user intervention is required at this step.

Designs for manufacturing are also specified in a very simple manner, using the click of a button. The Design for Manufacturing (DFM) option displays a dialog box similar to that in figure 5-4. This dialog box enables the user to select a number of simulation runs to perform. In the text box, STADIUM CKT informs the user of what type of design will be implemented based on the number of variables and the number of runs which has been selected. The user will also be informed if an improper number of runs has been selected to perform a valid set of simulations. In addition, properties of the design such as its strengths and weaknesses will be given.
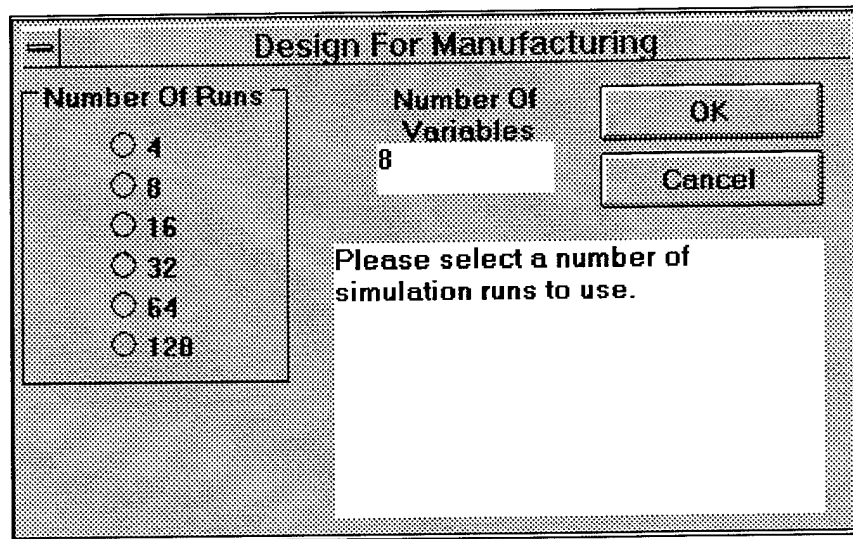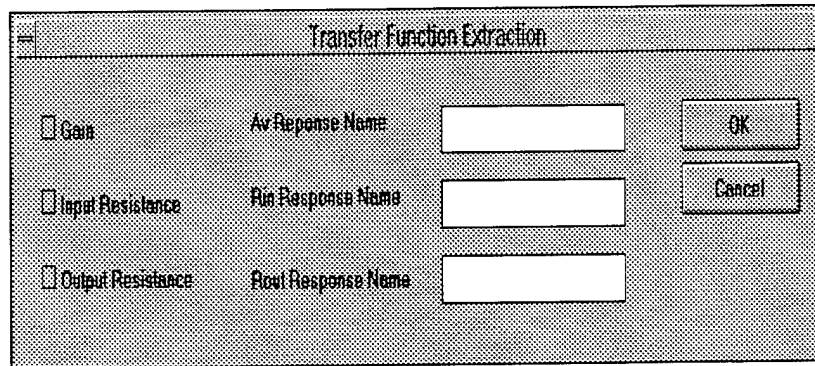

Figure 5-4 Design For Manufacturing

5.4 Output Data Extraction

Following the running of multiple PSpice simulations, important output data must be extracted from the Spice output files which were generated. This data is termed response data, and includes such things as transfer function gain, input resistance, and transient analysis rise or fall times. Though this data could be extracted by the user reading each output file, STADIUM CKT extracts this data automatically and easily generates the proper response files automatically. Many different types of data extraction are available depending on the specific type of analysis which was performed. Only two types of extraction will be shown here, the relatively simple extraction of transfer functions, and the more complicated and powerful extraction of transient analysis data.

The Transfer Function Extraction option (See Figure 5-5) allows the user to extract gain, input resistance and output resistance for the output variable defined in the transfer

function analysis specification dialog box. Response names for each of these outputs may be specified by the user. When the OK button is clicked the proper data will be extracted from the PSpice output file for each simulation run.
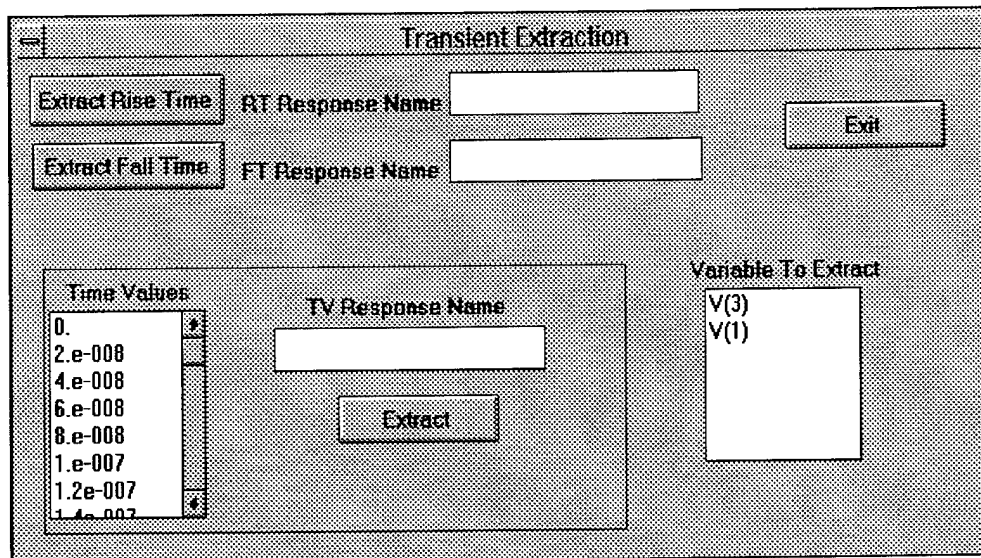

Figure 5-5 Transfer Function Extraction

When the user selects Transient Extraction a dialog box shown in Figure 5-6 appears.

Figure 5-6 Transient Extraction

This option allows the user to extract voltage or current values at specified times, as well as to extract rise and fall times for specified voltages or currents. To extract a voltage or current value select the desired time in the Time Values list box, select a node voltage or

branch current, assign it a name and click the Extract button. To extract rise and fall times, select a node voltage or branch current, assign a name and click on the appropriate extract button. STADIUM CKT will extract the rise time on the leading edge and the fall time on the lagging edge. Again, it is seen that STADIUM CKT makes easy work of a sometime tedious and error prone task.

5.5 Statistical Analysis

Statistical analysis involves the taking of a response file and knowledge of the type of design which was performed, then calculating statistical modeling information. This information in general takes two forms, one for a screening design and another for a DFM design. Both types of analysis are performed automatically simply by opening a response file and then with the click of a button telling STADIUM CKT to calculate the statistical information. Sample outputs from a screening design and a DFM design can be seen in figures 5-7 and 5-8 respectively.

```
Plackett-Burman Screening
Analysis

Factor Contributions:
RC1R   :        0.11 %
RC2R   :        0.11 %
P3NPNBF     :        23.68 %
P3NPNVA     :        29.39 %
P3PNPBF     :        26.54 %
P3PNPVA     :        20.17 %
```

Figure 5-7 Screening Design

As shown in figure 5-7, the relative factor contributions are given for all of the input variables. Typically after performing a screening design all those variables which are found to contribute less than 5% to the output response are turned off.

```
Fractional Factorial Analysis

Y = -62.152779 + (0.0187833)P3NPNBF +
(15.6059)P3NPNVA + (2.22386)P3PNPBF +
(22.225)P3PNPVA
Rsq = 0.996542
Estimated Mean = 3192.806641
Estimated Standard Deviation = 231.584201
Factor Contributions:
P3NPNBF      :        0.00 %
P3NPNVA      :       76.74 %
P3PNPBF      :        0.23 %
P3PNPVA      :       23.03 %
```

Figure 5-8 Fractional Factorial Design

Figure 5-8 shows the model which is developed for the output response. This model can then be used by the user in minimizing or maximizing a particular response. In addition the estimated mean response value is given followed by the estimated standard deviation. It should be noted that figures 5-7 and 5-8 were generated from different input data.

STADIUM CKT provides an easy and straightforward method of performing statistical circuit simulation. While all the steps in the process have not been covered, the major points in the process have been explained pointing out the ease of use which STADIUM CKT provides. STADIUM CKT truly gives even the novice statistics person a powerful tool in the development of statistical circuit models. Using this tool can be invaluable in the manufacturing process of complicated integrated circuits when taking into account the variability of manufacturing effects.

6. Technology Transfer and SOI Statistical Models

At the beginning of the Phase I contract, AET recognized that one of its most important tasks would be to develop a software technology which can be transferred to and would be used by the Low Power Electronics program community. Part of the issue of technology transfer is the ability to achieve valid statistical SOI models. In general, this can only be achieved by modeling real manufacturing processes and comparing the modeling results with real manufacturing data.

At this time, very little statistically valid manufacturing variability data exists on SOI transistors. This is especially true for the fully-depleted SOI (FDSOI) devices because they are quite new to the manufacturing environment. However, AET has formed partnerships with Lincoln Labs and SEMATECH to develop valid statistical FDSOI device experimental data and to compare this with simulation data. Specific details of the Lincoln Labs and SEMATECH partnerships will be discussed later in this section.

Modeling SOI processes and devices has proven to be a very difficult task. Part of the reason for this is that the SOI process and device physics are not as well understood as the physics for bulk devices. However, AET believes that this problem can be solved to a large degree by using the standard simulators (SUPREM and PISCES) with a statistical simulation methodology. The AET president, Dr. Thomas Sanders, has over 25 years of integrated circuit process and device experience and both Lincoln Labs and SEMATECH have committed to aid AET in the modeling activity.

One of the major issues investigated by the AET team is the dependence of the device electrical parameters on the variation of the active silicon layer thickness. A typical fully-depleted SOI transistor needs a silicon layer thickness of about 1000A. Working devices have been reported with silicon layers between 500A to 1500A. The manufacturing tolerance of + or - 200A has been found by some researchers to be far greater than can be tolerated for most processes. The threshold voltage control is not acceptable today and will get even worse when very low power supply voltages are used. The goal of the AET work is to determine the dependence of threshold voltage on the manufacturing process variations and to help derive the parameters for a high yield SOI process.

A very important subtask of this program has been the development of a structured methodology for deriving the statistical model information for the SOI transistor simulations. What is needed is manufacturing data concerning the statistical variations of all the important process steps in the integrated circuit fabrication. In principle, the measurement of this data is straightforward, but it is complicated by the fact that the number of manufacturing steps used to fabricate an SOI integrated circuit is very large (over 100 steps). This means that the statistical problem which must be solved is very complex and very difficult. What is required is a methodology for determining which of the process variables are important in the variation of the SOI transistor parameters and which are not. This process is called screening.

In the Phase I SBIR project, we have investigate alternative techniques for deriving this statistical information. We anticipate that a variety of techniques will ultimately be used. This includes methods such as fractional factorial design of experiments, sensitivity analysis, and engineering judgment.

6.1 Lincoln Labs Modeling Support

The Massachusetts Institute of Technology Lincoln Laboratories (Lincoln Labs) is a highly respected research organization near Lexington, MA. They employ several thousand personnel who are active in a wide variety of world class research and development projects. Microelectronics research is a major activity at Lincoln Labs. This

research is conducted in a modern 10,000 square foot clean room which has all the capability for fabrication of complex VLSI silicon chips as well as a wide variety of advanced semiconductor devices.

Lincoln Labs has for a long time been a leader in new semiconductor technology development. Many of these advanced devices have been developed for military applications and many Lincoln Labs devices are used in modern military equipment. Charge Coupled Devices (CCDs) for special applications have traditionally been a leading technology produced by Lincoln Labs. To support the CCD activity, Lincoln Labs has developed the worlds best capability in small geometry optical photolithography. Using 193 nanometer eximer laser radiation, Lincoln Labs has developed equipment, materials and a process to produce integrated circuit geometries down to 180 nanometers (0.18 microns).

This advanced photolithography technology has also made Lincoln Labs a leader in low power integrated circuits. With their new silicon-on-insulator technology called LPSOI, Lincoln Labs has become one of the leading labs in the country in advanced SOI processes. LPSOI can combine the benefits of fully-depleted SOI transistors with the high speed achieved by using polysilicon gate lengths of only 0.18 microns. At the present time, this LPSOI process is not optimized for either performance or for producibility in manufacturing. AET believes that by working with Lincoln Labs and the software STADIUM-LP, the optimized LPSOI process can be achieved faster than by any other method.

The leader of the Lincoln Labs microelectronics activity is Dr. Dave Shaver. Dr. Shaver has expressed a strong interest in working with AET and STADIUM-LP, as shown in the letter of support included as an attachment with this proposal. AET's Dr. Tom Sanders visited Lincoln Labs in June of 1995 and conducted technical discussions on the STADIUM statistical methodology. These discussions resulted in AET performing statistical simulations using STADIUM on the Lincoln Labs process data. A sample of this statistical simulation result is presented in Table 7-1.

The technical interactions between AET and Lincoln Labs have primarily taken place between AET's Mark Phelps and Lincoln Labs' Dr. Jim Burns. They have exchanged technical data and continue to work together to achieve accurate statistical models for the LPSOI technology. Dr. Burns supplied Mark Phelps with all the detailed process and device information relevant to the LPSOI technology including measured data and/or estimates of the manufacturing variations normally seen in the Lincoln Labs wafer fabrication line.

The actual process and device simulation was performed by Mark Phelps using the STADIUM-SOI in the computer lab at Florida Institute of Technology. Mark is a Ph.D. student at Florida Institute of Technology and expects to receive his degree in December 1995. He has been the primary researcher at the university and performed much of the software development work on STADIUM-SOI.

The simulation work on the LPSOI technology continues at this time. A preliminary report has been written on this STADIUM-SOI simulation activity. The results show good agreement between the STADIUM-SOI results and the Lincoln Labs data for the n-ch transistors but unsatisfactory agreement for the p-ch transistors. Mark Phelps is continuing to work with Dr. Jim Burns to achieve good agreement on all devices.

Table 7-1. Simulated Statistical Results for the Lincoln Labs SOI Process

Process/Device Parameter	Simulated Results	Experimental Results
N-ch Transistor Threshold Voltage	0.51volts	0.50volts
N-ch Transistor Threshold Voltage One Standard Deviation Variation	0.043volts	Data Not Available *
Percent Contribution to Variation of N-ch Transistor Threshold Voltage		Data Not Available *
-Gate Oxidation Temperature	56%	
-Active Layer Thickness	35%	
-All Other Process Variables	9%	

* Note that obtaining experimental data is proposed for the Phase II SBIR contract.

Lincoln Labs has already committed to being a beta site for the STADIUM-SOI. Installation of the software at Lincoln Labs is scheduled to take place in the middle of September. AET intends to work closely with Lincoln Labs for a number of months to be sure that the STADIUM software creates an accurate representation of the statistical variations of the Lincoln Labs LPSOI technology. AET has committed to be available to Lincoln Labs for training sessions on the use of STADIUM-SOI and will probably participate with Lincoln Labs in the design of special test mask structures, which are intended to be used to collect statistical LPSOI data.

6.2 Partnerships with IBM and SEMATECH

IBM at Yorktown Heights, New York, has for a long time been one of the country's leading producers of integrated circuits for high performance computers. Recently, IBM has been put under contract with ARPA to develop SOI technology for the Low Power Electronics. The initial discussions between IBM and AET started in March, 1995. As discussed in section 3.1 above, the initial technical person contacted at IBM by AET is Dr. Tom Theis. Dr. Theis has indicated possible problems with obtaining detailed process information from IBM. However, since he indicated that IBM does not spend a lot of time looking at process windows, STADIUM might be very useful for the process integration staff.

Subsequent technical discussions have been held with IBM's Erik Harris. Mr. Harris has been sent all relevant information about the AET SBIR Phase I contract and about the software STADIUM-SOI. IBM has reviewed this material and have concluded that at this time they are not ready to utilize STADIUM-SOI because they are not far enough along in their program to effectively use the statistical methodology in the tool. However, AET

will continue to work with IBM with the intention of having them evaluate STADIUM-SOI in the near future.

SEMATECH is the third major partner which AET has developed for its Low Power Electronics program. SEMATECH has been formed by a consortia of United States semiconductor companies for the purpose of advancing pre-competitive manufacturing technology for the integrated circuit industry. SEMATECH is located in Austin, Texas, and employs several hundred on its technical staff.

Dr. P. K. Vasudev, Program Manager at SEMATECH, has already made a commitment to work with AET on the Low Power Electronics program. SEMATECH was the funding source for the initial research work on the statistical simulation technology and have maintained a long term interest in its commercialization. In July of 1995, AET personnel presented a STADIUM course at SEMATECH, which was well received. As a result of this course, STADIUM will probably become an important part of the new technology development at SEMATECH.

SEMATECH will also provide the opportunity to establish one or more additional beta sites for STADIUM. We certainly expect that one beta site will exist with Dr. P. K. Vasudev in Austin. Since SEMATECH is run by a consortia of semiconductor companies, we fully expect that some of these companies will become interested in and want to evaluate the STADIUM software. These companies may also become beta sites which would give STADIUM a very wide audience and a cadre of reviewers.

AET expects to be able to provide some engineering support to all of the beta sites established. However, due to the time and money constraints, we do not expect to be able to support the SEMATECH member company beta sites to the same degree and completeness that we plan to support the Lincoln Labs and IBM beta sites.

6.3 Partnerships with Other Organizations

AET has recently developed a partnership with the engineers at Mayo Clinic in Rochester, MN. Dr. Barry Gilbert has consented that his department would be an evaluator of the STADIUM software. The plan is to install the STADIUM-SOI package at Mayo and participate with them in an evaluation of various Low Power Electronics processes. This process began at the end of the Phase I contract and will continue into the Phase II SBIR contract.

Besides the organizations mentioned above, there are a whole range of potential customers which AET has already contacted, and who may become beta sites for the STADIUM-LP software. Some of the organizations are members of SEMATECH, but many are not. This section of the proposal describes the interactions AET has had with them which indicates the contact and the nature of the potential application which each may have.

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7. Optimization Methodology

One of the tasks of the Phase I contract was the study of optimization techniques for SOI technologies. In optimizing a process, the user will determine the manufacturing equipment settings which both increase the product's resiliency to variation in the working environment while simultaneously moving the product to a desired set of parameters. These desired parameters (or responses) may be either a minimum (e.g. power), maximum (e.g. gain), or a target value (e.g. a threshold voltage of 0.35 V). No matter how the parameter is to be set, obtaining a minimum parameter variance is crucial for an optimized process.

7.1 SOI Technology Optimization Study

Too much variation degrades the quality of the product and causes a loss. Historically, the approach to this problem has been to set up upper and lower specification limits (USL and LSL) and perform inspections on finished products. If the product falls within the specification limits, no loss is assumed and the product is sold, whereas if the product lies outside the specification limits, the product is thrown away. Figure 7.1 illustrates that loss is based on the number of products produced outside these specification limits.
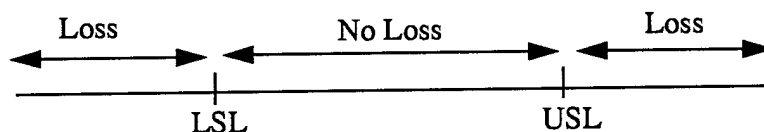

Figure 7.1: Historic Approach of Product Loss

There has been much work done in the area of statistical process control to reduce the number of products being produced outside the specification limits. This has resulted in most of the product lying within the specification limits. However, in the area of low power electronics, advanced architecture and design techniques have resulted in a strong relationship between manufacturing variations and circuit performance. This requires that the product's circuit parameters be tightly distributed about their desired value. This is accomplished through optimization. In optimizing the product's process, manufacturing equipment settings will be determined such that circuit parameters will have a minimum variance and centered about their target values. Figure 7.2 illustrates the difference between an optimized process and a non-optimized process.
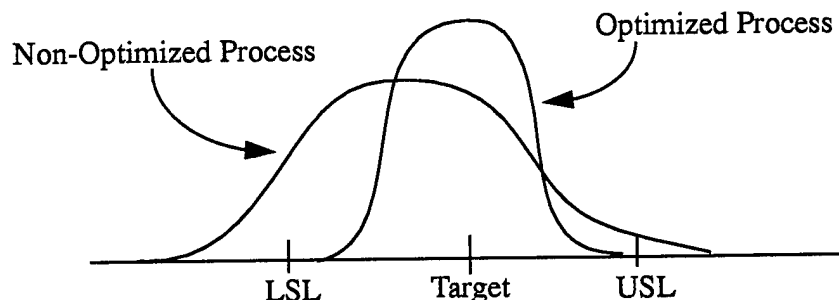

Figure 7.2: Optimized vs. Non-optimized Processes

In order to optimize a process, a statistically valid mathematical relationship between the input manufacturing variables and the product's response must be determined. This relationship is called a regression equation and is found by performing a statistical design of experiment. STA-DIUM was initially developed for the purpose of obtaining these regression equations and using them to statistically estimate the mean (or average) and variance of the response. STADIUM's existing design of experiments methodologies and statistical analysis capabilities provide a solid platform for extending into SOI technology optimization.

Taguchi designs have been used to aid the experimenter in process optimization. The purpose of experimentation using Taguchi's methodology is to identify those factors that have the greatest contribution to variation and to ascertain those settings or values that result in the least variability. They have proven effective because of their straightforward implementation and easily under-stood statistical metrics. Taguchi advocates that a single parametric function contains information about the manufacturing parameters that effect the location and the variance of the response. This function is called the signal-to-noise ratio with signal referring to the response's location and noise referring to the response's variation. There are separate signal-to-noise ratios for maximiz-ing, minimizing, or hitting a target value. The implementation of Taguchi designs is well suited to the TCAD environment because of the straightforward calculation and evaluation of the signal-to-noise ratios.

We have discovered, however, that other techniques may be developed that would give greater insight into the manufacturing process and provide more comprehensive optimization. For exam-ple, Taguchi designs do not provide any information regarding two-factor interactions. Even though two-factor interactions are often less important than main factors, their inclusion in a regression model could result in a much better model that "fits" the data more accurately. Signal-to-noise ratios do not distinguish factors that affect only the location of the response from factors that affect only the variance of the response. Nor do they distinguish those factors that affect both the location and variance of the response.

From the set of manufacturing factors, we must identify a subset of factors that affect the response's location and a subset of factors that affect the response's variance. Once these subsets of factors have been identified, the optimization procedure is relatively straightforward. This is shown in Figure 7.3. First, the factors that affect the variance are set to minimize the variance (b), then the factors which affect the location are set such that the response is centered over its target value (c).
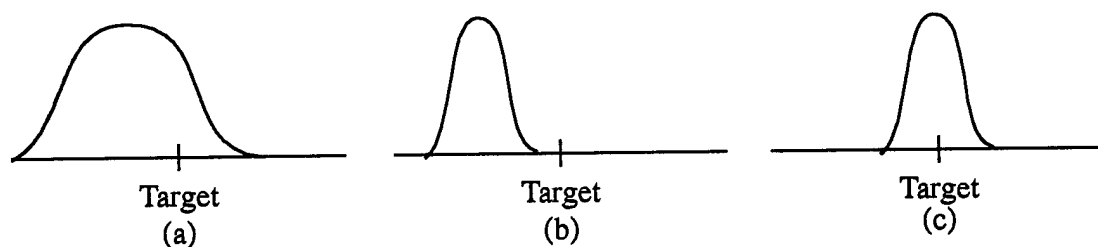

Figure 7.3: Procedure for Optimizing the Response

In every design optimization application, the response's variance is of vital interest to the experimenter. Thus, one very important characteristic of an optimized product is the ability to obtain a regression model for the variance. Obtaining a variance model is trivial in a physical experiment where each experimental run is repeated to produce a slightly different result. These repetitions are called "replecations" and are used to calculate a variance for each run of the experiment. These variances are then modeled as are the other responses. However, when deterministic simulators are used, replecations become meaningless. We have investigated several methods of creating statistically valid simulator replecations for the purpose of obtaining a regression model for the variance. These methods will be developed for STADIUM-LP (the software to be developed in the Phase II SBIR contract) and verified using data supplied by beta site partners.

It is possible that in order to optimize a process, manufacturing variables must be set at values outside the range of the experiment. By obtaining a regression model for the response, it is possible to use the model to determine those optimum variable settings, but unfortunately, polynomials are untrustworthy when extrapolated. Thus, a polynomial should be regarded as an approximation to the response only within the region bounded by the experiment. Response Surface Techniques (RSM) involves techniques for extending beyond the initial experimental region. We have investigated how RSM techniques may be developed for STADIUM-LP in cases where the optimum manufacturing settings lay beyond the initial experimental range.

The greatest challenge in the development of these optimization methodologies is to create a simulation environment that utilizes powerful statistical tools while providing the user with an intuitive, friendly interface. STADIUM has demonstrated that statistical complexities become transparent to the user when using design of experiments methodologies to estimate means and variances. We propose to leverage this level of user-intuitiveness into SOI technology optimization.

7.2   Development of SOI Optimization Capability

The development of an SOI optimization capability involves the development of three specific sub-systems. These sub-systems will be integrated with each other as well as with other STADIUM-LP sub-systems. The three sub-systems that are to be developed specifically for SOI optimization are the Statistical Design Generator, the Statistical Analysis, and the Sequential Statistical Control sub-systems.

The Statistical Design Generator sub-system has been previously developed for use in STADIUM-SOI in such a way that new designs may be easially added. Additionsl designs will be added such that STADIUM-LP will support the following experimental designs

    a. 2 level full factorial designs

    b. 3 level full factorial designs

    c. Fractional factorial designs of resolution III, IV, and V

    d. Plackett-Burman designs

    e. Central Composite designs

    f. Box-Behnken designs

g. Taguchi designs

h. Monte Carlo random variables

These designs will be generated automatically by STADIUM-LP and the user will be prompted through the graphical user interface when making a design choice. To eliminate some of the statistical complexity assiciated with choosing a design, the user simply chooses the number of runs he or she can afford to run and STADIUM-LP creates the design and informs the user as to what may be obtained from the design.

To investigate process robustness through optimization, many statistical analysis techniques must be implemented. Their statistical basis and complexity often make their use prohibitive by engineers with little or no background in statistics. We will implement many of the classical statistical analysis techniques in an intuitive graphical interface that will enable the user to evaluate the results of a statistical experiment. The user will be able to obtain the following:

a. Estimated mean and variance of the response

b. Regression models of the response vs. the input factors

c. Regression models of the response's variance vs. the input factors

d. Factor contributions (in percentages) to the variance of the response.

e. Plots of averages

f. Pareto charts

g. Normal probability plots

h. Calculation of Cp and Cpk

i. Contour plots

As stated in section 7.1, the variance of the response is of vital interest, and obtaining a model for the variance is an important component in optimization. Replecations are not possible using process and device simulators, so an alternative method has been developed to "simulate" replecations. Simply adding noise to each simulation run will produce slightly different results and may be thought of as a replecation, but unless this noise was added specifically from a noise factor in the outer array of a Taguchi design, we would be simply adding noise for the sake of adding noise and would not be able to determine any statistical information on how the factora affect the variance of the response. We have developed a technique that uses data from an unreplecated design to obtain the equivalent of valid statistical replecations.

As shown in Figure 7.4, we begin by performing the most suitable design based on n factors. From these n factors we next identify a subset of m factors that affect the response's location and obtain a regression model relating the response to the n factors. From the regression model, we obtain residuals (the difference between the fitted and simulated values) for each run. For each factor, we then calculate the variance of the residuals when the factor is set at its high leval and the variance of the residuals when the factor is set at its low levels. If the natural log of the ratio of these two variances is found to be significant, the factor is said to affect the response's variance. The significance of the ratio is determined using a probabilistic significance test. This is explained in more detail in reference. The result of this analysis is the identification of a subset of l factors

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that affect the variance. Next, identify the factor, p, that has the least affect on the variance but does affect the location. Reruning each run of the design with p at its oposite level will produce two values of the response for the same levels of the l factors affecting the variance. A variance is calculated from these two values and modeled as a function of the l factors.
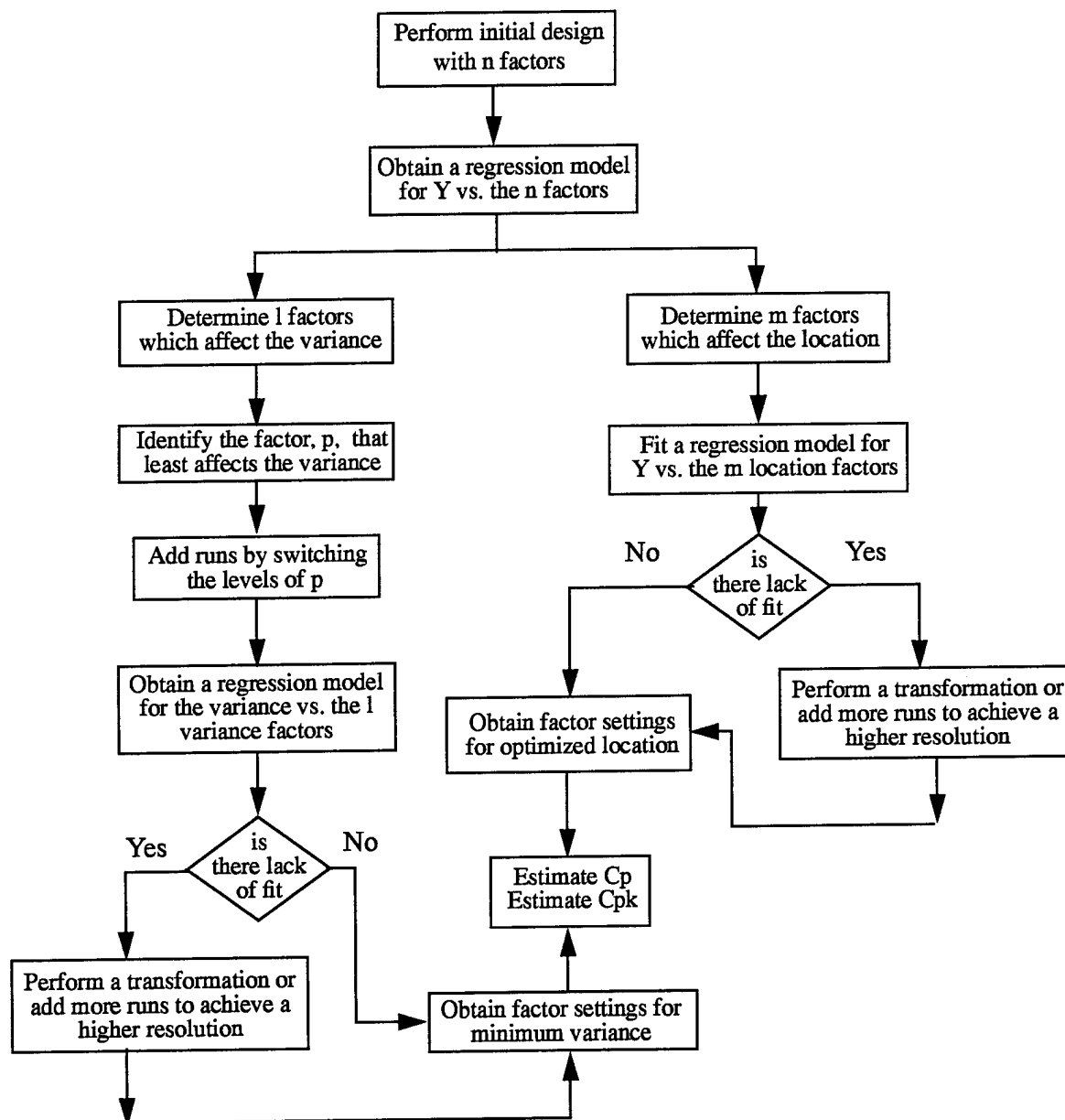
Perform initial design with n factors

Obtain a regression model for Y vs. the n factors

Determine l factors which affect the variance

Determine m factors which affect the location

Identify the factor, p, that least affects the variance

Fit a regression model for Y vs. the m location factors

Add runs by switching the levels of p

No   is there lack of fit   Yes

Obtain a regression model for the variance vs. the l variance factors

Obtain factor settings for optimized location

Perform a transformation or add more runs to achieve a higher resolution

Yes   is there lack of fit   No

Estimate Cp Estimate Cpk

Perform a transformation or add more runs to achieve a higher resolution

Obtain factor settings for minimum variance

Figure 7.4: Optimization Procedure

In many situations, the first experiment in the optimization procedure is a screening experiment. Usually, a fractional factorial design of resolution III is performed and the factors that affect the response's location are determined. Those factors that do not affect the location are then discarded and a subsequent experiment is performed to further investigate the important factors.

When the unimportant factors have been discarded, we are left with a new (or often called projected) design. It is possible that this new design has a higher resolution than the initial design of resolution III. If so, no runs are required to further investigate the factors. If the new design does not have a higher resolution, we should only need to run those factor settings that would give us a design of the next highest resolution when combined with the new design.

To accomplish this, we have developed techniques to identify the statistical resolution of a fractional factorial design and to compare it to designs of higher resolution with all possible confounding patterns. This enables the user to save many extra simulation runs.

This sequential methodology will be implemented into STADIUM-LP. The user will be prompted by intuitive graphic user interfaces while the statistical analysis is performed internally.

8. Other Program Activities

During this SBIR program, there has been a number of activities for the contract which have not reported upon above. These consist of trips to ARPA in Washington, DC and contacts made with potential users of the STADIUM-SOI product software to be developed during Phase II of this program. In addition, several technical paper abstracts have been submitted for conference publications.

The first visit to ARPA on this program occurred on March 10, 1995. This was a meeting between the ARPA Program Manager, Zachary Lemnious, and the AET Principal Investigator. The purpose of the meeting was to discuss the details of the program plan proposed by AET. The ARPA program manager was very helpful in spelling out some of the critical needs of the Low Power Electronics program. As a result of this program, a detailed program plan was generated and delivered to ARPA in March 1995.

The second major interaction activity was participation in the ARPA Low Power Electronics Program Review which occurred outside Washington, DC on April 27 and 28, 1995. This review was attended by over 100 researchers and government officials. The AET principal investigator gave one of the presentations at this meeting. This presentation consisted of overview information about the STADIUM general technology as well as specific information about the plans and results of the SBIR program. A complete set of viewgraphs presented at this review are included in the Appendix of this report.

On July 31, 1995 another meeting was held at ARPA between Program Manager, Zachary Lemnious, and the AET Principal Investigator. This meeting consisted of a review of the program results as of that date as well as a discussion of potential tasks that would be appropriate for a Phase II SBIR program.

AET, has also been in contact with a number of companies besides IBM who may be eventual users of the STADIUM-SOI system. Our plan is to remain in contact with these companies so that the system that is finally developed by AET will meet the needs of most industrial users.

Interactions with Motorola in Austin, Texas have taken place in a number of ways. Work has started with Mike Mendicino, a Motorola Assignee at SEMATECH, to begin using STADIUM this fall. This may be the quickest use of the technology outside the program described above with Lincoln Labs. Also, at Motorola, we have had discussions with Joe Nahas on low power electronics circuit design. In addition, we have presented STADIUM to Ken Jones of Motorola for use as a yield enhancement tool in their SOI and bulk manufacturing lines.

Rockwell International has also expressed broad interest in STADIUM and its capability to statistically simulate SOI devices. A number of interactions have taken place with Jerry Brandewie, who is a Rockwell assignee at SEMATECH. He has indicated that several Rockwell people in California are interested in evaluating STADIUM. Recently, contacts have been made with Zef Shanfield in Anaheim, who has been involved in the low power program at Rockwell.

Honeywell in Plymouth, MN, is interested in using the STADIUM methodology in their SOI technology development. Initial discussions have taken place with Jerry Yue (device modeling) and Jerry Grauley (marketing). More recently, we have had discussions with James Lai, who is directly involved in statistical simulation of Honeywell's SOI technologies.

Texas Instruments in Dallas has been visited several times by AET personnel. The primary focus of STADIUM at TI has been with Ted Houston. In addition, Harold Hosack, a

technology development manager, has invited a discussion of STADIUM to be given at a special workshop on statistical methods in integrated circuits. This workshop is sponsored by SEMATECH in Austin. TI has been using different versions of STADIUM for several years and will probably be one of the users of STADIUM-LP for SOI work.

Other companies have also been contacted concerning the use of STADIUM for SOI device modeling. One of these is Loral in Manassas, Virginia where Fred Brady and Jon Maimon have been briefed. Also, contacts have been made with Wade Crule and other engineers at Ibis. They have participated with AET in supplying statistical SOI silicon thickness data to aid in the STADIUM-SOI test cases run.

Several interactions have also taken place with agencies of the United States government. The National Security Agency has indicated a desire to secure a copy of an earlier version of STADIUM for aiding their understanding of the integrated circuit process. Specific contacts include Rathindra Pal and Russ Jones of the NSA Reliability section. Also, Peter Roitman of the National Institute of Science and Technology has been interested in and received information about the STADIUM-SOI software.

9. Conclusions

AET, Inc. believes that this Phase I SBIR proposal has been quite successful. All of the stated contract deliverables have been completed on schedule and all program goals have been achieved. AET has demonstrated the ability to not only achieve excellent technical results but also to develop partnerships which will help make the overall ARPA Low Power Electronics program successful.

The most fruitful partnerships developed to date include those with Lincoln Labs and SEMATECH. Both of these organizations have made a commitment to utilize STADIUM in their R&D work. As discussed above, AET has also presented STADIUM to a number of potential low power electronics companies. The ability to build these relationships demonstrates that AET is the kind of organization that not only can develop useful software but will also make sure that the customers are ready to employ the technology.

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Appendix A

**Presentation for ARPA at the
Low Power Electronics Review
Reston, VA
April 27, 1995**

Statistical Modeling of SOI Devices for the Low Power Electronics Program

Tom Sanders
Principal Investigator
AET, Inc. Melbourne Florida

ARPA Contract No. DAAH01-95-C-R031   AET, Inc.

Presentation Overview

- **Program Objectives/Approach/Status**
  - **-STADIUM Software Prototype**
  - **-Statistical SOI Modeling**
  - **-Optimization Concepts**
- **STADIUM Overview**
- **STADIUM Example**
- **Conclusions and Summary**

ARPA Contract No. DAAH01-95-C-R031   AET, Inc.

STADIUM Overview

- STADIUM is a software shell which drives existing smulators to make them easy to use and more productive.
- It employes Design of Experiments methodology to derive statistical information.
- Almost any simulator can be integrated into the STADIUM envirnoment.
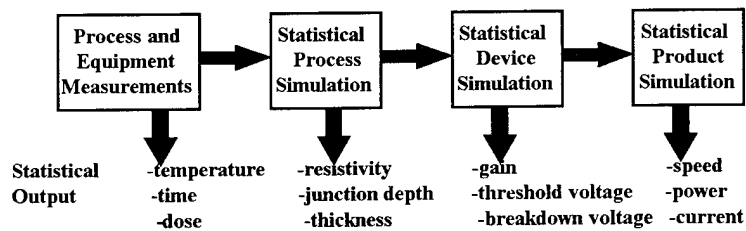
AET, Inc.

History of STADIUM Technology

- Initial DFM work at Florida Tech began in 1989 with funding from the State of Florida.
- STADIUM software research began in 1990 with funding from SEMATECH.
- In 1992, Texas Instruments began funding special industrial applications of STADIUM.
- Today, STADIUM work continues with SEMATECH, TI and other organizations.
- In 1994, AET, Inc. was formed to support and commercialized the STADIUM software.

AET, Inc.

STADIUM METHODOLOGY FOR STATISTICAL SIMULATION OF INTEGRATED CIRCUITS

Process and Equipment Measurements	Statistical Process Simulation	Statistical Device Simulation	Statistical Product Simulation

Statistical Output	-temperature -time -dose	-resistivity -junction depth -thickness	-gain -threshold voltage -breakdown voltage	-speed -power -current

ARPA Contract No. DAAH01-95-C-R031

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Benefits of STADIUM DoE Methodology

- **Reduces the number of simulations required.**
- **Uses screening to identify significant variables.**
- **Can obtain response surfaces for the results which are valid over the range of input variation. These are mathematical relationships which relate the results to the significant variables.**
- **Can determine the relative importance of the inputs in determining the variance of the results.**
- **Leads to design optimization through RSM and Taguchi techniques.**

ARPA Contract No. DAAH01-95-C-R031

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Statistical Simulation Example

The STADIUM software performs statistical simulation on IC processes as described in this simple example.
Assume there is an CMOS process flow which has a number of process steps, each of which have some statistical variation. It is desired to determine how each of these process variations affect the variation of the N-ch transistor threshold voltage (Vt).
STADIUM is ideally suited for this task

Statistical Simulation Input Data

To develop the input data for the statistical simulation, the process flow is inspected for all possible steps which could have variations affecting the threshold voltage. Below are listed eleven process variables considered.

- P-well implant energy and dose
- P-well diffusion time and temperature
- Gate oxide growth time and temperature
- Vt adjust implant energy and dose
- Gate photoresist length dimension
- Source/drain anneal time and temperature

Typical STADIUM Results

STADIUM outputs data in the form of estimates of process and device parameter means and standard deviations. An example result for a CMOS technology is presented below.

Threshold Voltage Mean Value = 0.530 volts
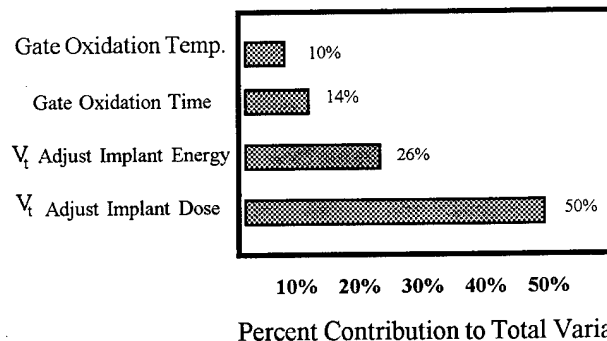*Threshold Voltage Standard Deviation = 0.047 volts*

A chart is produced which gives the contribution of each important process step to the total variation of each output parameter as shown on the next slide.

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STADIUM Results Showing the Percent Contributed to the Threshold Voltage Variance by Four Process Variables

Gate Oxidation Temp.	10%
Gate Oxidation Time	14%
V_t Adjust Implant Energy	26%
V_t Adjust Implant Dose	50%

10%   20%   30%   40%   50%

Percent Contribution to Total Variance

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Appendix B

Statistical Modeling Report for
MIT Lincoln Laboratories
Lexington, Mass.
July, 17, 1995

Preliminary Statistical Simulation Report on the Low Power Silicon-On-Insulator (LPSOI) MOS Process

**Prepared for MIT's Lincoln Laboratories
by AET, Inc. & Florida Institute of Technology
Thomas J. Sanders & Mark J. Phelps**

Contents

1.0 Project Overview

Two SOI MOS devices, described by Silvaco's Athena process simulator files, were received via email from Jim Burns at Lincoln Laboratories on Wednesday, July 5, 1995 (Section 2.1). Initial simulations using Silvaco Tools were performed to reproduce the simulation results as previously performed at Lincoln Laboratories. Next, the simulation flows were re-entered using STADIUM-SOI's Process Specification Menus and Automated Gridding routines to insure appropriate gridding for use in statistical simulation. Nominal (single run with no input variation) simulations were performed to insure that the simulations represented qualified devices. Thirty-five variables were identified as possible sources of input variation (Section 2.2) and a screening methodology was used to determine the important factors, those that contribute to at least 1% of the variation in the output response. Finally, statistical models were calculated using linear regression analysis. The experiment was then repeated under the assumption that none of the input variation was due to the starting wafers (i.e. the variations in the starting SOI wafers were "turned off") and statistical models were again calculated.

2.0 LPSOI MOS Experiment

Two devices, NMOS and PMOS, were modeled.

UNITS: Time: minutes | Temperature: degrees Celsius | Concentration: atoms/cm^2 | Thickness: microns | Pressure: atmospheres | Energy: KeV

* denotes the value was used as a source of input variation; ** set to the same level

2.1 LPSOI MOS Process Flow

0.) Starting Wafer: Substrate concentration: 7.5e14* at/cm2 Boron orientation: 100

0.6u* Active Layer, doping concentration: 5e14* at/cm2 phosphorous

0.4u* Buried Oxide Layer

1.) Diffusion time=30* temp=825* dryo2 pressure=1.00*

2.) Diffusion time=10* temp=825* nitrogen pressure=1.00*

3.) (NMOS) Implantation BF2 dose=3.5e12* energy=20* pearson tilt=10

   (PMOS) Implantation Phosphorus dose=2e12* energy=25* pearson tilt=10

4.) Etch oxide all

5.) Diffusion time=15* temp=900* dryo2 pressure=1.00*

6.) Diffusion time=10* temp=900* nitrogen pressure=1.00*

7.) Deposition polysilicon thickness=0.3* phosphorus concentration=1e14*

8.) Etch polysilicon*

9.) Diffusion time=30* temp=850* dryo2 pressure=1.00*

10.) Diffusion time=10* temp=850* nitrogen pressure=1.00*

11.) (NMOS) Implantation Arsenic dose=5e14* energy=25*

12.) (PMOS) Implantation BF2 dose=5e14* energy=25*

13.) Deposition oxide thickness=0.15**

14.) Etch oxide dry thickness=0.15**

15.) (NMOS) Implantation Arsenic dose=5e15* energy=30* pearson

(PMOS) Implantation BF2 dose=5e15* energy=30* pearson

16.) Diffusion time=0.7* temp=1000* dryo2 pressure=0.25*

17.) Metallization

2.2 Process Flow Input Variations

Wafer start variations were determined from "best case" Ibis Technology General Product Specification Sheets as of August 1, 1995 (Standard SIMOX process).

Note: Factor screening and statistical modeling was also performed without the starting wafer variations under the general assumption that the starting wafers were "perfect" and therefore not a source of input variation. (Sections 2.3.3 & 2.4.3)

SOI Layer Variation: Lot-to-lot Uniformity (+/- 5nm) + On Wafer Uniformity (8nm)
==> Total SOI variation=13nm

Buried Oxide Variation: Lot-to-lot Uniformity (+/- 5nm) + On Wafer Uniformity (10nm)
==> Total BOX variation = 15nm

The following were provided by Jim Burns, Lincoln Laboratory:

Parameter	Sigma/Mean	Data Source
Temperature	.012	10nm Gate Oxide Tests
Time	.012	10nm Gate Oxide Tests
Doping	.005	Implanter Dose Control Specification
Poly Thickness	.075	Recent CMOS Runs
LPCVD Oxide Thickness	.075	Recent CMOS Runs

The remaining variations were estimated as reasonable values to be used, pending receipt of data to the contrary.

Parameter	Sigma/Mean
Implant Energy	0.03
Lithography	0.05
Diffusion Pressure	0.03

2.3 LPSOI NMOS Experiment

2.3.1 LPSOI NMOS Nominal Experiment

The NMOS SOI device was simulated (Figs 1-5) with the following results:

Channel Length: 0.21 (um)

Threshold Voltage: 0.55 (V)

Gain: 2.57E-05 (A/um-V)

Subthreshold slope: 74.96 (mV/dec)

These target values may differ from empirical results since the process has not been "tuned" to meet the unit process steps. Since implant profile and diffusion steps are the main contributors to the differences between simulation and experimental data, study of intermediate steps in the actual process leading to adjustment of distributions and diffusion coefficients may lead to more exact results. Since we are looking for statistical process trends, this tuning process is usually less critical. The identification of important process steps can, and often is, clearly identified without the adjustment of the simulation target (response variable) to meet the experimental results. However, if one is provided with process data at intermediate stages, this procedure can be repeated with a tuned process flow which may improve the accuracy of the results.
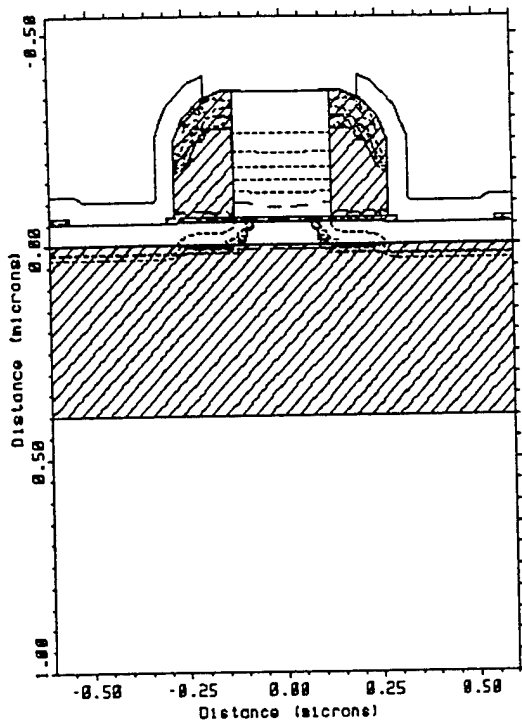
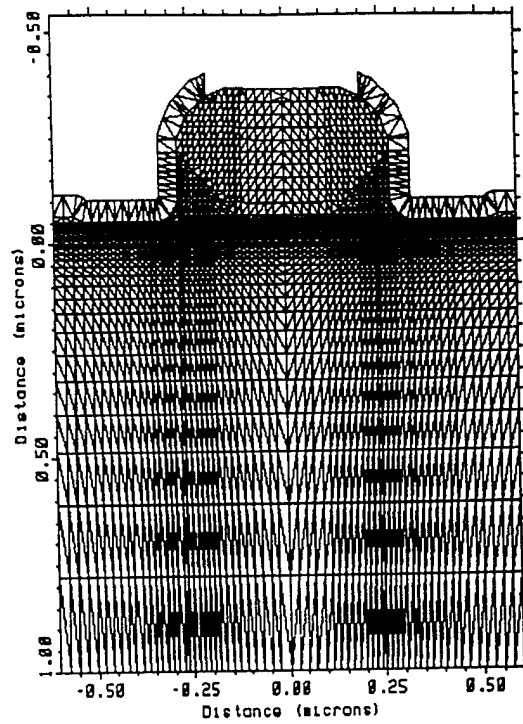FIGURE 1. SOI NMOS Cross Section

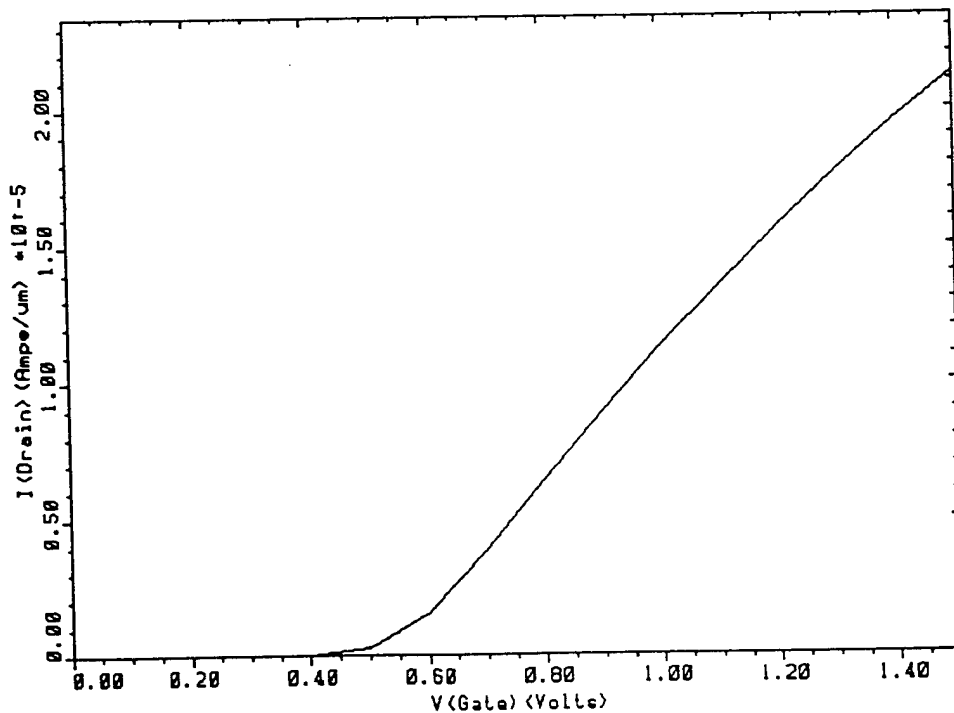FIGURE 2. Simulation Grid

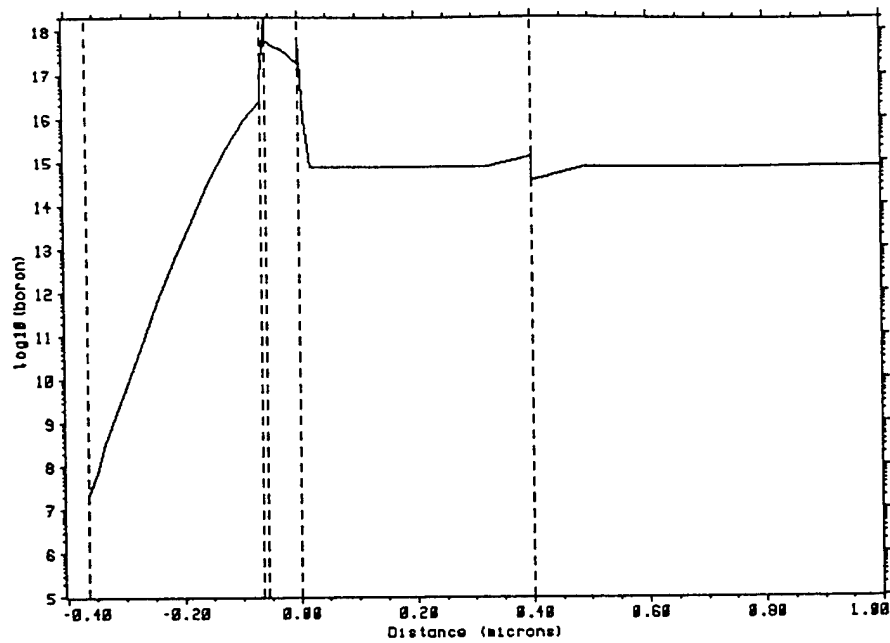FIGURE 3. SOI NMOS I(Drain) vs. V(Gate)

FIGURE 4. Doping Profile through the gate region @x=0 (P-type)
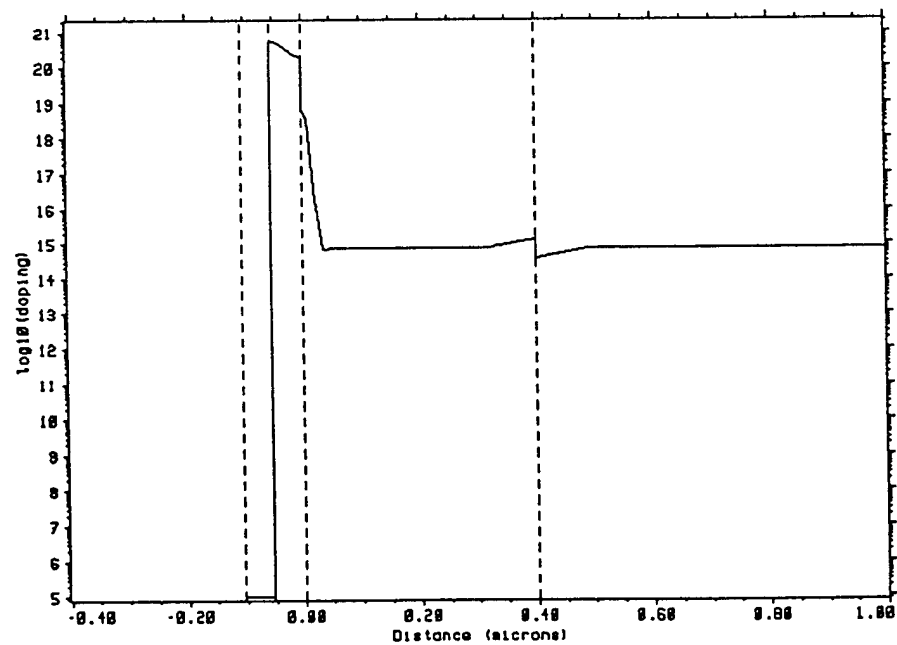

FIGURE 5. Doping Profile through the S/D Regions @x=0.35 (N-type)

2.3.2 LPSOI NMOS Modeling Experiment with Wafer Variation

The process flow (Section 2.1) was simulated with 35 input variations (Section 2.2) identified using a plackett-Burman 36 run design. The factors shown in Table 1 were determined to be important for threshold voltage, transconductance (gain), and subthreshold slope.

TABLE 1. LPSOI NMOS Factors Identified as Important to the Response Parameters (#): Step in Section 2.1 and the Corresponding Percent of Contribution to the Variation in the Output Response

Threshold Voltage	%	Transconductance	%	Subthreshold Slope	%
Gate Oxide Temperature (5)	56.25	Polysilicon Lithography (8)	46.50	Gate Oxide Temperature (5)	40.05
Active Layer Thickness (0)	34.86	Gate Oxide Temperature (5)	44.61	Active Layer Thickness (0)	37.06
N+ Contact Implant Drive-In Temperature (16)	3.78	Active Layer Thickness (0)	8.59	Polysilicon Lithography (8)	20.57
Polysilicon Lithography (8)	3.53			N+ Contact Implant Drive-In Temperature (16)	1.49
Initial Oxide Temperature (1)	1.58				

Once the important factors are identified, the response modeling is performed. The goal of the modeling experiment is to mathematically relate the response to the input factors in the form of an equation. This model allows for the estimation of the response at levels other than those used in the experiment. This model is the basis upon which the estimated mean and variance of the response is calculated. This equation relates the response (often referred to as Y 'hat" where hat denotes that the response is estimated) to each of the factors. A more complex equation may be obtained by including interaction terms but were not needed here because the Rsq values were shown to be close to 1. Rsq is often referred to as the proportion of the variability in the data that is accounted for by the model. Clearly, the closer Rsq is to 1, the more response variation is accounted for and the model may be viewed as accurate.

Threshold Voltage (Vt)

$Vt = -4.5 + (-8.53e\text{-}4)init\_oxide\_temp + (4.66e\text{-}4)gate\_ox\_temp$

$\quad + (2.02)poly\_litho + (1.09e\text{-}2)cont\_imp\_drive\_temp + (3.05)silicon\_thickness$

Rsq = 0.977

Estimated Mean = 0.51 V

Estimated Standard Deviation = 6.72e-2 V

Transconductance (gm)

$gm = 1.99e\text{-}4 - (3.92e\text{-}09)init\_oxide\_temp - (1.58e\text{-}07)gate\_ox\_temp$

$- (2.79e\text{-}4)poly\_litho + (1.13e\text{-}08)cont\_imp\_drive\_temp - (5.76e\text{-}05)silicon\_thickness$

Rsq = 0.994

Estimated Mean = 2.6e-5 A/um-V

Estimated Standard Deviation = 3.0 e-6 A/um-V

Subthreshold Slope (S)

$S = -71.64 - (2.74e\text{-}2)init\_ox\_temp + (0.17)gate\_ox\_temp$

$- (215.70)poly\_litho + (0.03)cont\_imp\_drive\_temp$

$+ (139.19)silicon\_thickness$

Rsq = 0.964

Estimated Mean = 74.2 mV/dev

Estimated Standard Deviation = 2.97 mV/dec

2.3.3 LPSOI NMOS Modeling Experiment without Wafer Variation

The process flow (Section 2.1) was simulated with 22 input variations (Section 2.2) identified using a plackett-Burman 24 run design. The factors shown in Table 2 were determined to be important for threshold voltage, transconductance (gain), and subthreshold slope.

TABLE 2. LPSOI NMOS Factors Identified as Important to the Response Parameters (#): Step in Section 2.1 and the Corresponding Percent of Contribution to the Variation in the Output Response

Threshold Voltage	%	Transconductance	%	Subthreshold Slope	%
Gate Oxide Temperature (5)	90.70	Polysilicon Lithography (8)	53.21	Gate Oxide Temperature (5)	63.58
Polysilicon Lithography (8)	5.32	Gate Oxide Temperature (5)	46.45	Polysilicon Lithography (8)	32.70
N+ Contact Implant Drive-In Temperature (16)	3.98			N+ Contact Implant Drive-In Temperature (16)	3.72

Threshold Voltage (Vt)

$Vt = -5.06 + (4.91e-3)gate\_ox\_temp + (2.06)poly\_litho + (9.27e-4)con\_drive\_temp$

$Rsq = 0.999$

Estimated Mean = 0.55 V

Estimated Standard Deviation = 5.58e-2 V

Transconductance (gm)

$gm = 1.85e-4 - (1.5e-07)gate\_ox\_temp + (2.79e-4)poly\_litho + (1.17e-08)con\_drive\_temp$

$Rsq = 0.996$

Estimated Mean = 2.6e-4 A/um-V

Estimated Standard Deviation = 2.0e-6 A/um-V

Subthreshold Slope (S)

$S = -107.43 + (0.19)gate\_ox\_temp - (234.41)poly\_litho + (0.041)con\_drive\_temp$

$Rsq = 0.978$

Estimated Mean = 74.68 mV/dec

Estimated Standard Deviation = 2.56 mV/dec

2.4 LPSOI PMOS Experiment

2.4.1 LPSOI PMOS Nominal Experiment

The PMOS SOI device was simulated (Figs 6-10) with the following results:

Channel Length: 0.16 (um)

Threshold Voltage: -1.50 (V)

Gain: 1.44E-05 (A/um-V)

Subthreshold slope: 67.47 (mV/dec)
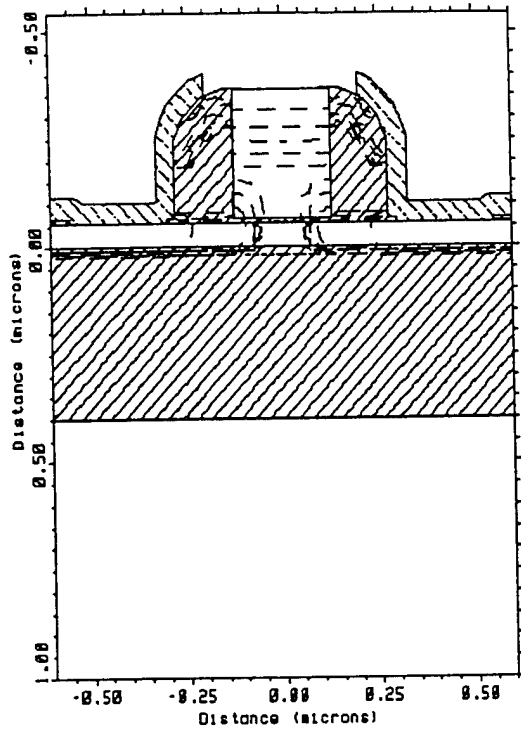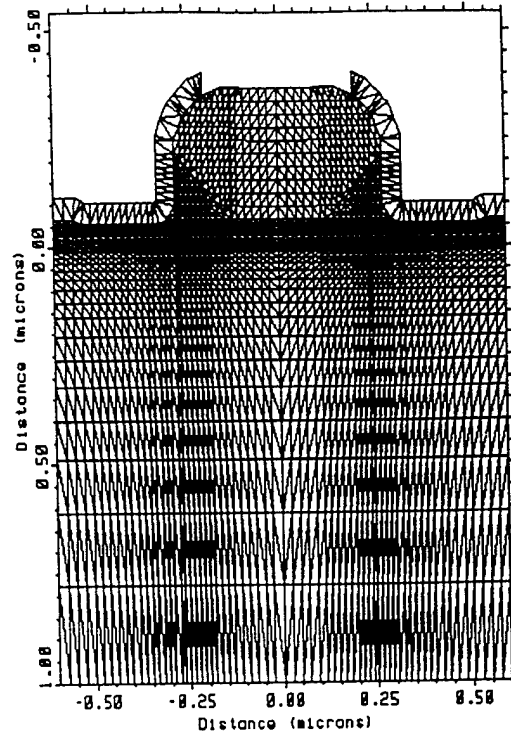
FIGURE 6. SOI PMOS Cross Section
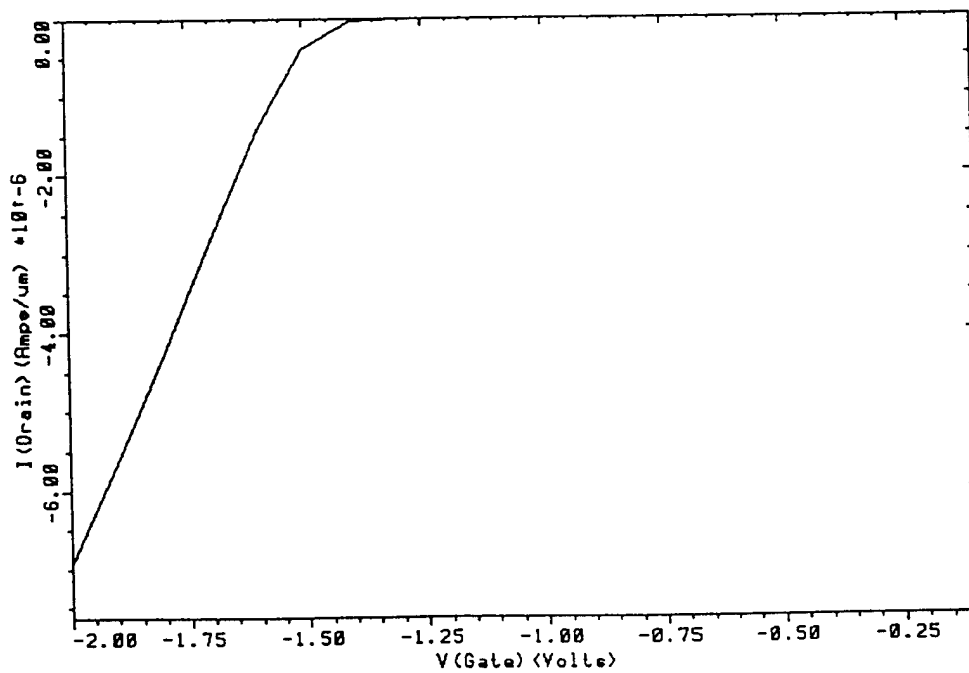

FIGURE 7. Simulation Grid

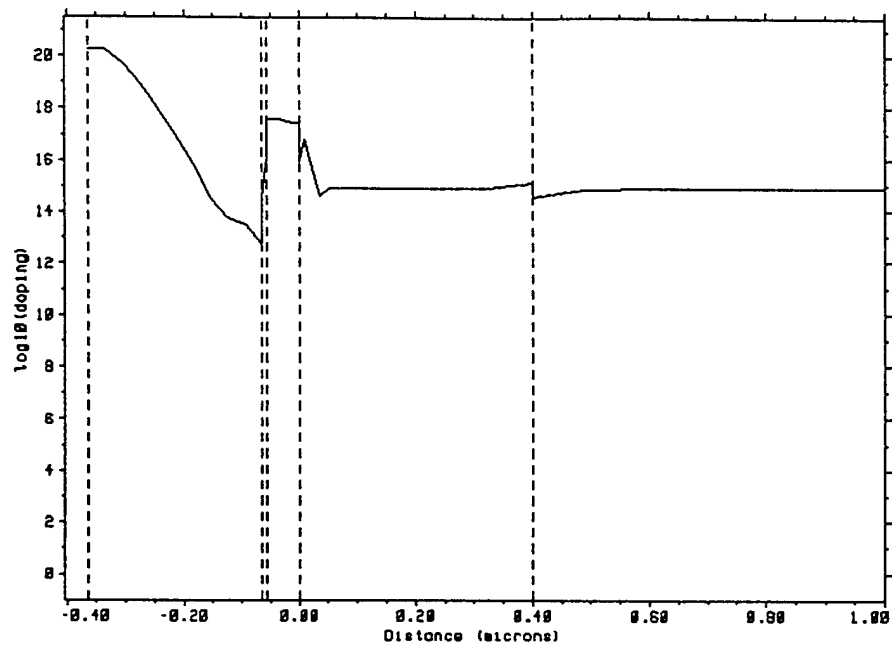

FIGURE 8. SOI PMOS I(Drain) vs. V(Gate)

FIGURE 9. Doping Profile through the gate region @x=0 (N-type)
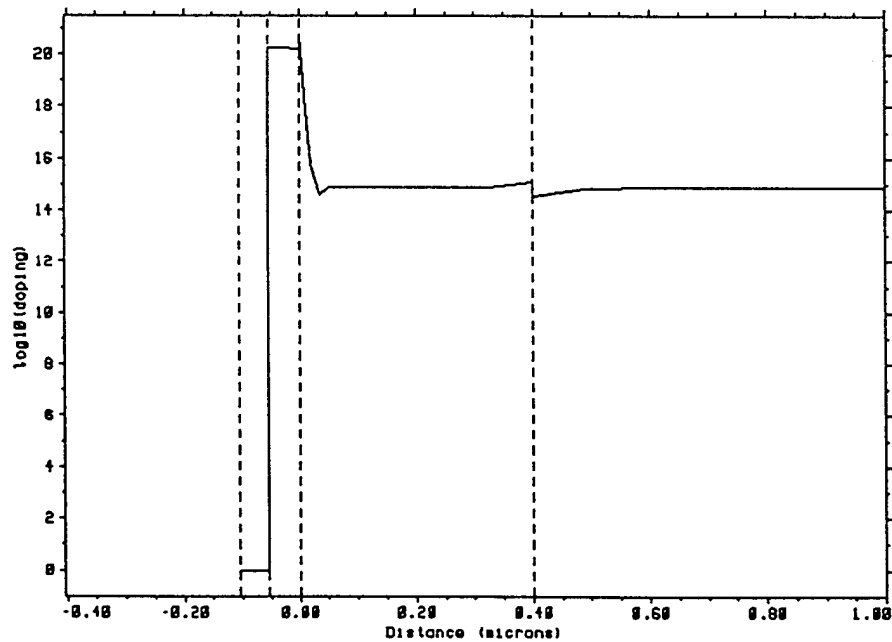

FIGURE 10. Doping Profile through the S/D Regions @x=0.35 (P-type)

2.4.2 LPSOI PMOS Modeling Experiment with Wafer Variation

The process flow (Section 2.1) was simulated with 35 input variations (Section 2.2) identified using a Plackett-Burman 36 run design. The factors shown in Table 3 were determined to be important for threshold voltage and transconductance (gain). An accurate model for subthreshold slope was not obtained for this case because certain combinations of input variables caused the shape of the output curve to be such that consistent extraction of the subthreshold slope proved difficult. Although a model was calculated, its Rsq value was significantly low enough (~0.2) to consider its fit insufficient.

TABLE 3. LPSOI PMOS Factors Identified as Important to the Response Parameters (#): Step in Section 2.1 and the Corresponding Percent of Contribution to the Variation in the Output Response

Threshold Voltage	%	Transconductance	%
Gate Oxide Temperature (5)	76.93	Gate Oxide Temperature (5)	55.43
Polysilicon Lithography (8)	10.39	Polysilicon Lithography (8)	29.42
N+ Contact Implant Drive-In Temperature (16)	7.62	N+ Contact Implant Drive-In Temperature (16)	14.12
Active Layer Thickness (0)	5.06	Active Layer Thickness (0)	1.02

Threshold Voltage (Vt)

$Vt = 2.57 - (5.95e\text{-}3)gate\_ox\_temp - (3.78)ploy\_litho$

$+ (1.68e\text{-}3)con\_drive\_temp + (1.26754)silicon\_thickness$

Rsq = 0.989

Estimated Mean = -1.50 V

Estimated Standard Deviation = -0.073 V

Transconductance (gm)

$gm = 0.000105 - (1.51e\text{-}07)gate\_ox\_temp - (1.90e\text{-}4)poly\_litho$

$+ (6.86e\text{-}08)con\_drive\_temp + (1.70e\text{-}05)silicon\_thickness$

Rsq = 0.990

Estimated Mean = 1.50e-5 A/um-V

Estimated Standard Deviation = 2e-6 A/um-V

2.4.3 LPSOI PMOS Modeling Experiment without Wafer Variation

The process flow (Section 2.1) was simulated with 22 input variations (Section 2.2) identified using a plackett-Burman 24 run design. The factors shown in Table 4 were determined to be important for threshold voltage, transconductance (gain), and subthreshold slope.

TABLE 4. LPSOI NMOS Factors Identified as Important to the Response Parameters (#) and the Corresponding Percent of Contribution to the Variation in the Output Response

Threshold Voltage	%	Transconductance	%	Subthreshold Slope	%
Gate Oxide Temperature (5)	79.37	Gate Oxide Temperature (5)	54.87	Gate Oxide Temperature (5)	75.68
Polysilicon Lithography (8)	11.99	Polysilicon Lithography (8)	30.32	N+ Contact Implant Drive-In Temperature (16)	24.01
N+ Contact Implant Drive-In Temperature (16)	8.64	N+ Contact Implant Drive-In Temperature (16)	14.81	Polysilicon Lithography (8)	0.31

Threshold Voltage (Vt)

$Vt = 2.58 - (5.96e\text{-}3)gate\_ox\_temp - (3.99)poly\_litho + (1.77e\text{-}3)con\_drive\_temp$

Rsq = 0.999

Estimated Mean = -1.51 V

Estimated Standard Deviation = -0.072 V

Transconductance (gm)

$gm = 1.02e\text{-}4 - (1.48e\text{-}7)gate\_ox\_temp - (1.9e\text{-}4)poly\_litho + (6.92e\text{-}8)con\_drive\_temp$

Rsq = 0.996

Estimated Mean = 1.40e-5 A/um-V

Estimated Standard Deviation = 2.0e-6 A/um-V

Subthreshold Slope (S)

$S = -745.57 + (0.58)gate\_ox\_temp + (63.57)poly\_litho + (0.29)con\_drive\_temp$

Rsq = 0.621 (not considered a very "good" fit)

Estimated Mean = 76.94 mV/dec

Estimated Standard Deviation = 7.19 mV/dec

3.0 Conclusions

Both the NMOS and PMOS devices were statistically modeled. The nominal characteristics, since they were not tuned to empirical data, may need to be adjusted to more accurately represent the process flow. Despite this, the model trends should provide valuable insight into the effects of fabrication variations on the device yield. Upon receipt of more detailed and current process data, these experiments will be repeated in an effort to improve the manufacturability of the designs. We look forward to continued cooperation with Lincoln Laboratories and hope that our efforts contribute to the success of your research.

Appendix C

**Program Review Presented to
Zachary Lemnious at ARPA
Washington DC
July 31, 1995**

Statistical Modeling of SOI Devices for the Low Power Electronics Program

AET, Inc.
Melbourne Florida

Research Team
Tom Sanders, PI
Mark Phelps, Associate PI
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Eric Schlanger

ARPA Contract No. DAAH01-95-C-R031   **AET, Inc.**

Contract Deliverables

1. Prototype Software Development
   - STADIUM™ SOI for Transistor Modeling.
   - Statistical SOI Circuit Simulation Methods.
2. Technology Transfer to Low Power Electronics Program Partners
   - Work with IBM, Lincoln Labs, IBIS and SEMATECH.
   - Develop Statistical Models of New Processes.
3. Study SOI Technology Optimization
   - Taguchi Techniques.
   - Response Surface Methods.

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What is STADIUM™ SOI?

1. STADIUM™ SOI is a software shell which drives commercial SUPREM-4 and PISCES simulators to make them easy to use and more productive for advanced SOI technology simulation.
2. STADIUM employs Design of Experiments methodology to derive statistical device electrical results from materials and process variations.
3. Almost any IC process simulator can be integrated into the STADIUM environment.

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Prototype Software Development Accomplishments

1. Completed STADIUM™ SOI Software Package for SOI Transistor Modeling.
2. Manual and Documentation for STADIUM™ SOI are near complete.
3. Plans are in place to install STADIUM™ SOI at Lincoln Labs and SEMATECH as Beta Sites.
4. Standalone Statistical Circuit Simulation Methods have been explored.

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Technology Transfer Accomplishments

1. IBM: Contacts made with Erik Harris and others. Process information not now available to AET.
2. Lincoln Labs: Have received complete SOI process info and have completed initial simulations. Dave Shaver has requested STADIUM™ SOI.
3. IBIS: Have included the IBIS material variations from Mike Alles in simulations for Lincoln Labs.
4. SEMATECH: Process flow used for initial SOI statistical simulations by AET. P. K. Vasudev has requested STADIUM™ SOI.

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SOI Optimization Methods Accomplishments

1. Taguchi methods have been identified as the initial optimization technique to obtain the best trade-off between hitting the design center point and reducing output variations.
2. Response Surface Methods is the advanced optimization technique to center the design outside the original design space.

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Plans to Complete the SBIR Contract

1. Deliver the STADIUM™ SOI software and documentation to ARPA.
2. Continue process modeling of Lincoln Labs and SEMATECH SOI processes.
3. Install STADIUM™ SOI at Lincoln Labs and possibly SEMATECH and IBM.
4. Complete and deliver the contract final report and the Phase II proposal to ARPA.

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Phase II SBIR Program Vision

1. Develop an advanced version of STADIUM called STADIUM™ LP (for LOW POWER) which is aimed directly at users of the ARPA Low Power Electronics Program technology.
2. The goal is for STADIUM™ LP to contain statistical models of the LPE technology developed by IBM, Lincoln Labs, or other organizations.
3. The low power technology can then be efficiently transferred to other companies by transferring STADIUM™ LP which is maintained by AET.

ARPA Contract No. DAAH01-95-C-R031   AET, Inc.

Phase II SBIR Proposal Summary
Principal Investigator: Mark J. Phelps
Proposed Duration: Two Years

Task Summary

1. STADIUM™ LP software enhancements and product development.
2. Implementation of optimization techniques into STADIUM™ LP.
3. Integration of other process simulators into the STADIUM™ LP environment.
4. Develop SOI reliability models for STADIUM
5. Technology Transfer to several organizations.

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Phase II, Task 1.
STADIUM™ LP software enhancements and product development.

1. Integration of process, device and circuit simulation capabilities for low power technologies.
2. Develop capability for automatic scaling of small geometry CMOS and SOI devices.
3. Complete STADIUM™ LP product development including documentation and users manual.

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Phase II, Task 2.
Implementation of optimization techniques into STADIUM™ LP.

1. Develop Taguchi optimization methods which will be compatible with STADIUM.
2. Investigate Response Surface Methods and Modeling the Variance techniques for integrated circuit optimization.
3. Integrate appropriate optimization techniques into STADIUM™ LP.

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Phase II, Task 3.
Integration of other process simulators into the STADIUM™ LP environment.

1. Investigate possible process and device simulators which could enhance the STADIUM™ LP capability. Search SRC, government and other sources for existing and emerging simulators.
2. Develop the STADIUM software needed to easily incorporate additional simulators into the environment.

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Phase II, Task 4.
Develop SOI reliability models for STADIUM

1. Develop hot electron injection models for the thin SOI gate oxides.
2. Develop electrostatic damage and related models for the sub-micron SOI devices.
3. Integrate appropriate SOI reliability models into STADIUM™ LP.

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Phase II, Task 5.
Technology Transfer of STADIUM™ LP.

1. Install STADIUM™ LP at Lincoln Labs and provide technical support to optimize their LPSOI process.
2. Support IBM, IBIS and SEMATECH to implement STADIUM™ LP methodologies.
3. Develop working relationships with commercial fabs (such as TI, Rockwell, Motorola and Honeywell) to install and use STADIUM™ LP.

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Summary of Goals for the Phase II SBIR Contract

1. Develop the existing prototype software into a robust STADIUM^{TM} LP product.
2. Facilitate a user base for STADIUM^{TM} LP among the ARPA Low Power Electronics Program community.
3. Meet advanced customer needs by developing customer directed enhancements to the basic STADIUM^{TM} LPsoftware.

ARPA Contract No. DAAH01-95-C-R031

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Cost Proposal

1. Base Program (4.5 man-years) - $375,000
Develop STADIUM^{TM} LP (Tasks 1, 2, 3 and 4)

2. Option Program (1.5 man-years) - $115,000
Technology Transfer of STADIUM^{TM} LP (Task 5)

Schedule

Two Years beginning January 1996

AET, Inc.

Appendix D

Paper presented at the
1995 IEEE International SOI Conference
October 3, 1995

SIMULATION OF THE EFFECTS OF MANUFACTURING PROCESS VARIATIONS ON THE CHARACTERISTICS OF SOI MOSFETS

T. J. Sanders, AET, Inc., and M. J. Phelps, Florida Institute of Technology
Melbourne, FL 32901

Successful scaling of SOI MOSFETs to deep sub-micron features for use in high density and low power applications will require a thorough understanding of the effect of process variation on device yield. Manufacturing steps that contribute most to device parameter variation must be identified so that tolerances can be tightened. This paper shows that Design of Experiments (DoE) methodology can be applied to commercial process and device simulation packages to gain insight into the process flow of SOI devices and to identify possible challenges to be met in the fabrication of future devices.

Previous work in this area has concentrated on setting device parameters (e.g., channel length) to attain an optimum threshold voltage (Vt) [1]. This is clearly the logical first step. However, the unit process step is the actual control point and design trade-offs will not allow a decision to be made solely on Vt. Instead, information involving many response variables and input variable interactions must be considered prior to the optimization of SOI manufacturing. With DoE, multiple input variables (factors) are screened to determine their contributions to the variation in the output response while minimizing the number of runs required [e.g., if the number of input variables (n) equals 20, the experiment requires 24 simulation runs using Plackett-Burman techniques vs. a 2 level full-factorial requiring more than a million (2^n)]. Once the important variables are identified, another DoE is applied to obtain a statistical model with main effects and variable interactions [e.g., the 10 remaining important variables require 16 to 64 runs based on the interaction terms desired].

In regard to the statistical model, it has been argued that the estimated mean of a simulation output is strongly dependent upon proper tuning of the simulator to the process flow. Regardless of tuning, the estimated standard deviation of the output response and input factor contributions to that output can still provide valuable information on process trends. Therefore, process and device simulation and its use in the design of high yield ICs can be greatly enhanced through the use of statistics. Indeed, as simulation models improve, DoE methodology will become all the more effective.

Statistical models of fully and partially depleted (FD & PD) MOSFETs were derived in an effort to complement the physical modeling work that is currently being done. No attempt was made to improve upon existing physical models, but rather to draw upon existing CAD tools to demonstrate the value added by using Design of Experiments.

Exact information on manufacturing variations of a product are proprietary. However, high volume semiconductor manufacturers strive to make all unit process variations conform to at least a three sigma value of no more than 5%. Based on this, reasonable estimates for unit step variation were obtained for the examples herein (Table 1). First, the fourteen factors shown in Table 1 were screened with a 20-run DoE and five factors for each device were found to be important. Next, statistical models were calculated for three output responses (Vt, gm, & subthreshold slope (S)) using 32-run Resolution V DoE. The resulting regression models are shown on the facing page along with the factor contributions (Figs 1-3) for each response.

The statistical data generated through this procedure can now be used to provide a better understanding of the process. For example, lithography and channel doping steps for the FD device are shown to be critical to the control of Vt, gm, & S and time & temperature steps to be less important. However, in the PD device, time & temperature factors dominate the effect on subthreshold slope. Quantifiable statistical information such as this useful in order to improve SOI device. Comparison with manufacturing data has demonstrated the usefulness of statistical data generated through the application of DoE to computer simulation.

[1] Hung-Sheng Chen and Sheng S. Li, "A Comparison of Statistical Variation of Threshold Voltage in Bulk Silicon and SOI MOSFETS", IEEE International SOI Conference, Vail Valley, CA, Oct. 1991.

Table 1: Process Step Values & Variations and Percent Contributions to Response Variation

Process Step	Values & Variations			Partially Depleted			Fully Depleted		
	Value	Variation	Units	Vt (%)	gm(%)	S (%)	Vt (%)	gm(%)	S (%)
Buried Oxide Thickness	3800	190	Å	0.95	0.70	7.46	0.10	0.00	0.98
Active Layer (SOI) Thickness	1500/750	75	Å	1.14	0.12	1.82	16.30	2.48	6.42
Active Layer (SOI) Doping	2e17	2e16	at/cm^2	37.17	12.60	10.10	58.52	16.13	36.18
Gate Oxide Time	5	0.25	min.	4.96	1.45	9.10	4.06	3.69	1.56
Gate Oxide Temperature	950°	5°	C	20.86	7.31	29.13	8.90	5.95	0.07
Poly Deposition Thickness	3000	150	Å	0.01	0.03	0.38	0.01	0.27	0.79
Poly Diffusion Time	30	1.5	min.	0.03	0.02	0.01	0.06	0.03	0.02
Poly Temperature	800°	5°	C	0.04	0.16	3.68	0.00	0.00	0.59
Poly Doping	1e20	1e19	at/cm^2	0.04	0.00	0.22	0.01	0.03	0.05
PR Gate/Poly Alignment		250	Å	20.98	52.40	19.70	8.52	48.86	32.61
S/D Implant Dose	4e15	2.8e15	at/cm^2	0.19	2.31	0.14	0.13	1.10	0.42
S/D Energy	45 / 35	1.35	KeV	0.14	0.10	0.65	0.01	0.12	1.53
S/D Diffusion Time	70 / 55	3.5	min.	2.44	4.03	4.98	0.60	3.69	5.49
S/D Diffusion Temperature	950°	5°	C	11.05	18.77	12.64	2.79	17.63	13.28

Statistical Models

Partially-Depleted SOI NMOS

Vt = -0.919 + (1.30x10^{-18})[SOI Doping]
+ (3.84x10^{-3}) [Gate Ox Temp] - (0.742)[PR Alignment]
- (2.67x10^{-3})[S/D Diff Temp] + (4.12x10^{-2})[Gate Ox Time]
Est. mean: 0.284 V| Est. std. dev: 4.08x10^{-2}

gm = -1.87x10^{-4} + (1.76x10^{-4})[PR Alignment]
+ (5.35x10^{-7})[S/D Diff Temp] - (1.16x10^{-22})[SOI Doping]
- (3.46x10^{-7})[Gate Ox Temp] - (3.12x10^{-6})[Gate Ox Time]
Est. mean: 4.20x10^{-5} A/um-V | Est. std. dev: 6x10^{-6}

S = -289.27 + (0.188)[Gate Ox Temp]
+ (0.167)[S/D Diff Temp] + (33.01)[PR Alignment]
+ (2.76x10^{-17})[SOI Doping] + (1.94)[Gate Ox Time]
Est. mean: 79.5 mV/decl Est. std. dev: 1.67

Fully-Depleted SOI NMOS

Vt = -1.085 + (1.40x10^{-18})[SOI Doping]
+ (4.07)[SOI Thickness] - (0.51)[PR Alignment]
+ (2.28x10^{-3}) [Gate Ox Temp] - (1.31x10^{-3})[S/D Diff Temp]
Est. mean: 0.165 V | Est. std. dev: 3.67x10^{-2}

gm = -2.08x10^{-4} + (1.68x10^{-4})[PR Alignment]
+ (5.24x10^{-7})[S/D Diff Temp] - (1.09x10^{-22})[SOI Doping]
- (3.06x10^{-7})[Gate Ox Temp] - (2.33x10^{-4})[SOI Thickness]
Est. mean: 4.40x10^{-5} A/um-V | Est. std. dev: 6x10^{-6}

S = -209.38 + (133.76)[PR Alignment]
- (1.64x10^{-16})[SOI Doping] + (0.414)[S/D Diff Temp]
- (475.60){SOI Thickness] - (0.113)[Gate Ox Temp]
Est. mean: 74.69 mV/decl Est. std. dev: 5.45

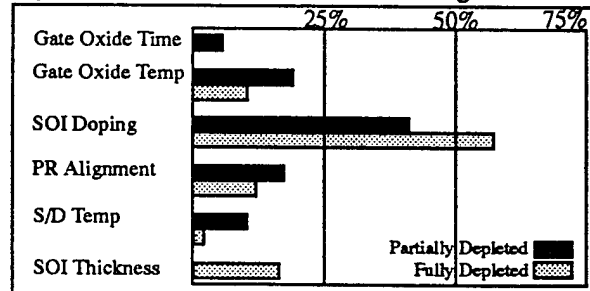Fig. 1. Factor Contribution to Threshold Voltage

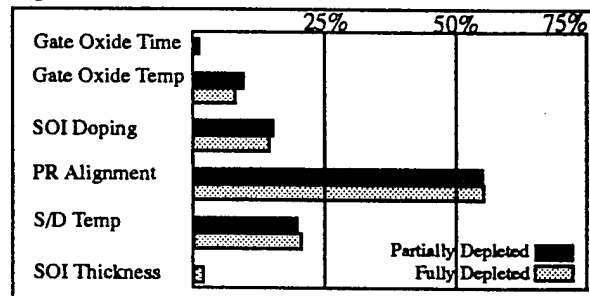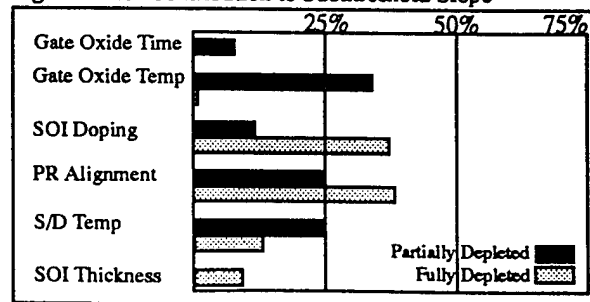Fig. 2. Factor Contribution to Transconductance

Fig. 3. Factor Contribution to Subthreshold Slope

Appendix E

Paper Submitted to the
1996 Government Microelectronics Applications Conference
Orlando. Florida
March 1995

STADIUM-SOI: STATISTICAL DESIGN FOR MANUFACTURING SOFTWARE FOR LOW POWER SILICON-ON-INSULATOR MOSFETS*

T. J. Sanders, AET, Inc., M. J. Phelps and G. T. Hess, Florida Institute of Technology

Melbourne, FL 32901

Abstract

Successful scaling of MOSFETs to deep sub-micron features for use in high density and low power applications will require a thorough understanding of the effect of process variations on device yield. Manufacturing steps that contribute most to device parameter variation must be identified so that tolerances can be tightened. This paper shows that Design of Experiments (DoE) methodology can be applied to commercial process and device simulation packages to gain insight into the process flow and to identify possible challenges to be met in the fabrication of future devices. The automated application of DoE to process and device simulation via a user-friendly (window environment) software package called STADIUM-SOI (Statistical Design for Manufacturing - Silicon On Insulator devices) is currently being developed for the ARPA Low Power Electronics program.

I. Introduction

STADIUM-SOI is a Technology-Computer-Aided-Design (TCAD) tool that combines the field of statistics with Silicon-On-Insulator (SOI) Integrated Circuit (IC) design. Computer simulation has the potential to improve IC chip yields only to the extent that the software is used. STADIUM will enable process and device engineers to include in their designs the effects of manufacturing variation on product yield.

Because time is so valuable, it is often the biggest obstacle one faces with respect to statistical computer simulation. First, most commercial software is hard to use and requires hours of practice before one has confidence in the results. Next, the total number of experimental design options is overwhelming and demands a great deal of time be spent studying statistics. Finally, the time involved in setting up and controlling a multiple (e.g. 32 run) DoE from the process to the device level, including correct structure and variable substitution, is prohibitive.

STADIUM-SOI provides a push-button windowing environment that eliminates the need to memorize complicated and often cryptic simulator syntax. Default process step models are chosen specifically for

SOI technology to optimize the accuracy of the simulations. Furthermore, statistical options are reduced to a complete set of default experiments. By following the logical progression of STADIUM's statistical design package, the engineer is led to develop a model of the response, estimated mean, estimated standard deviation, and factor contributions. The resulting statistical model is based on a response variable (e.g. threshold voltage) which will be comprised of statistically derived coefficients multiplied by the process step variations (e.g. channel doping).

In regard to the statistical model, it has been argued that the estimated mean of a simulation output is strongly dependent upon proper tuning of the simulator to the process flow. Regardless of tuning, the estimated standard deviation of the output response and input factor contributions to that output can still provide valuable information on process trends. Therefore, process and device simulation and its use in the design of high yield ICs can be greatly enhanced through the use of statistics. Indeed, as simulation models improve, DoE methodology will become all the more effective.

Section II provides an example of the application of DoE to process and device simulation, Section III briefly describes the functionality of STADIUM-SOI, and Section IV explains the statistical methodology employed in STADIUM-SOI.

II. Statistical Simulation of Partially and Fully Depleted SOI MOSFETS

As an example of the benefits of the coupling of DoE with simulation, statistical models of fully and partially depleted (FD & PD) MOSFETs are presented. No attempt was made to improve upon existing physical models, but rather to draw upon existing CAD tools to demonstrate the value added by using DoE methods.

Exact information on manufacturing variations of a product are proprietary. However, high volume semiconductor manufacturers strive to make all unit process variations conform to at least a three sigma value of no more than 5%[1]. Based on this, reasonable estimates for unit step variation were obtained for the examples herein (Table 1). First, the fourteen factors shown in Table 1 were screened (Tables 2 & 3) with a 20-run DoE and five factors for each device were found to be important. Next, statistical models were calculated for three output responses (Vt, gm, & subthresh-

old slope (S)) using 32-run Resolution V (Refer to Section IV) DoE. The factor contributions for each response (Figs. 1-3) and the resulting regression models are included herein.

The statistical data generated through this procedure can now be used to provide a better understanding of the process. For example, lithography and channel doping steps for the FD device are shown to be critical to the control of Vt, gm, & S and temperature steps to be less important. However, in the PD device, temperature factors dominate the effect on subthreshold slope.

Table 1: SOI NMOS Process Steps and Variations

Process Step	Value	Variation	Units
Buried Oxide Thickness	3800	190	Å
Active Layer (SOI) Thickness	1500/750	75	Å
Active Layer (SOI) Doping	2e17	2e16	at/cm^2
Gate Oxide Time	5	0.25	min.
Gate Oxide Temperature	950°	5°	C
Poly Deposition Thickness	3000	150	Å
Poly Diffusion Time	30	1.5	min.
Poly Temperature	800°	5°	C
Poly Doping	1e20	1e19	at/cm^2
PR Gate/Poly Alignment		250	Å
S/D Implant Dose	4e15	2.8e15	at/cm^2
S/D Energy	45 / 35	1.35	KeV
S/D Diffusion Time	70 / 55	3.5	min.
S/D Diffusion Temperature	950°	5°	C

Table 2: Partially Depleted NMOS Screening Results

Process Step	Vt (%)	gm(%)	S (%)
Buried Oxide Thickness	0.95	0.70	7.46
Active Layer (SOI) Thickness	1.14	0.12	1.82
Active Layer (SOI) Doping	37.17	12.60	10.10
Gate Oxide Time	4.96	1.45	9.10
Gate Oxide Temperature	20.86	7.31	29.13
Poly Deposition Thickness	0.01	0.03	0.38
Poly Diffusion Time	0.03	0.02	0.01
Poly Temperature	0.04	0.16	3.68
Poly Doping	0.04	0.00	0.22
PR Gate/Poly Alignment	20.98	52.40	19.70
S/D Implant Dose	0.19	2.31	0.14
S/D Energy	0.14	0.10	0.65
S/D Diffusion Time	2.44	4.03	4.98
S/D Diffusion Temperature	11.05	18.77	12.64

Table 3: Fully Depleted SOI NMOS Screening Results

| Process Step	Vt (%)	gm(%)	S (%)
Buried Oxide Thickness	0.10	0.00	0.98
Active Layer (SOI) Thickness	16.30	2.48	6.42
Active Layer (SOI) Doping	58.52	16.13	36.18
Gate Oxide Time	4.06	3.69	1.56
Gate Oxide Temperature	8.90	5.95	0.07
Poly Deposition Thickness	0.01	0.27	0.79
Poly Diffusion Time	0.06	0.03	0.02
Poly Temperature	0.00	0.00	0.59
Poly Doping	0.01	0.03	0.05
PR Gate/Poly Alignment	8.52	48.86	32.61
S/D Implant Dose	0.13	1.10	0.42
S/D Energy	0.01	0.12	1.53
S/D Diffusion Time	0.60	3.69	5.49
S/D Diffusion Temperature	2.79	17.63	13.28

Fig. 1: Factor Contribution to Threshold Voltage
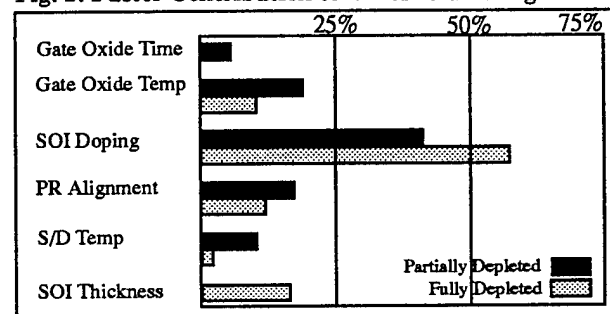
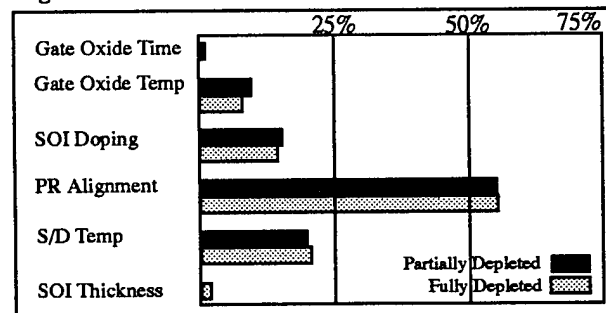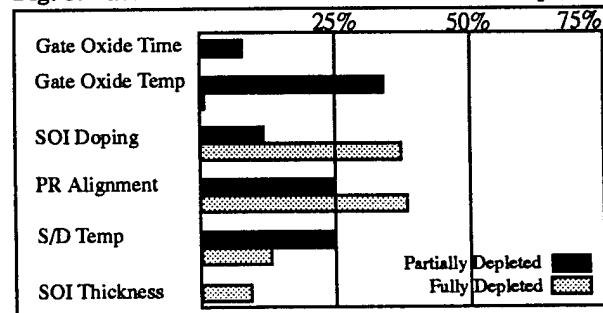Fig. 2: Factor Contribution to Transconductance

Fig. 3: Factor Contribution to Subthreshold Slope

Statistical Models:

Partially-Depleted SOI NMOS

$Vt = -0.919 + (1.30 \times 10^{-18})$[SOI Doping]
$+ (3.84 \times 10^{-3})$ [Gate Ox Temp] $- (0.742)$[PR Alignment]
$- (2.67 \times 10^{-3})$[S/D Diff Temp] $+ (4.12 \times 10^{-2})$[Gate Ox Time]
Est. mean: 0.284 V| Est. std. dev: 4.08×10^{-2}

$gm = -1.87 \times 10^{-4} + (1.76 \times 10^{-4})$[PR Alignment]
$+ (5.35 \times 10^{-7})$[S/D Diff Temp] $- (1.16 \times 10^{-22})$[SOI Doping]
$- (3.46 \times 10^{-7})$[Gate Ox Temp] $- (3.12 \times 10^{-6})$[Gate Ox Time]
Est. mean: 4.20×10^{-5} A/um-V | Est. std. dev: 6×10^{-6}

$S = -289.27 + (0.188)$[Gate Ox Temp]
$+ (0.167)$[S/D Diff Temp] $+ (33.01)$[PR Alignment]
$+ (2.76 \times 10^{-17})$[SOI Doping] $+ (1.94)$[Gate Ox Time]
Est. mean: 79.5 mV/dec| Est. std. dev: 1.67

Fully-Depleted SOI NMOS

$Vt = -1.085 + (1.40 \times 10^{-18})$[SOI Doping]
$+ (4.07)$[SOI Thickness] $- (0.51)$[PR Alignment]
$+ (2.28 \times 10^{-3})$ [Gate Ox Temp] $- (1.31 \times 10^{-3})$[S/D Diff Temp]
Est. mean: 0.165 V | Est. std. dev: 3.67×10^{-2}

$gm = -2.08 \times 10^{-4} + (1.68 \times 10^{-4})$[PR Alignment]
$+ (5.24 \times 10^{-7})$[S/D Diff Temp] $- (1.09 \times 10^{-22})$[SOI Doping]
$- (3.06 \times 10^{-7})$[Gate Ox Temp] $- (2.33 \times 10^{-4})$[SOI Thickness]
Est. mean: 4.40×10^{-5} A/um-V | Est. std. dev: 6×10^{-6}

$S = -209.38 + (133.76)$[PR Alignment]
$- (1.64 \times 10^{-16})$[SOI Doping] $+ (0.414)$[S/D Diff Temp]
$- (475.60)$\{SOI Thickness] $- (0.113)$[Gate Ox Temp]
Est. mean: 74.69 mV/dec| Est. std. dev: 5.45

Quantifiable statistical information such as this is useful to improve SOI device yield. Comparison with manufacturing data has demonstrated the usefulness of statistical data generated through the application of DoE to computer simulation.[2]

III. STADIUM-SOI

The application of DoE to process and device simulation has been automated in a user-friendly (window environment) software package called STADIUM-SOI (Statistical Design for Manufacturing - Silicon On Insulator devices) in a project supported by the Advanced Research Projects Agency (ARPA) for their Low Power Electronics program.

The STADIUM-SOI main menu (Figure 4) invokes four modules, Process Design, Simulation Control, Simulation Output, and Statistical Analysis. The relationship between these modules is shown in the block diagram in Fig. 5.
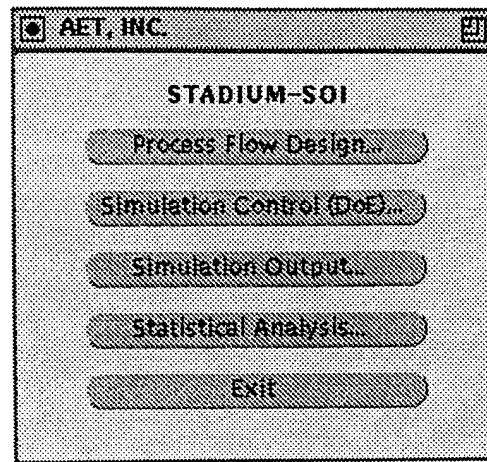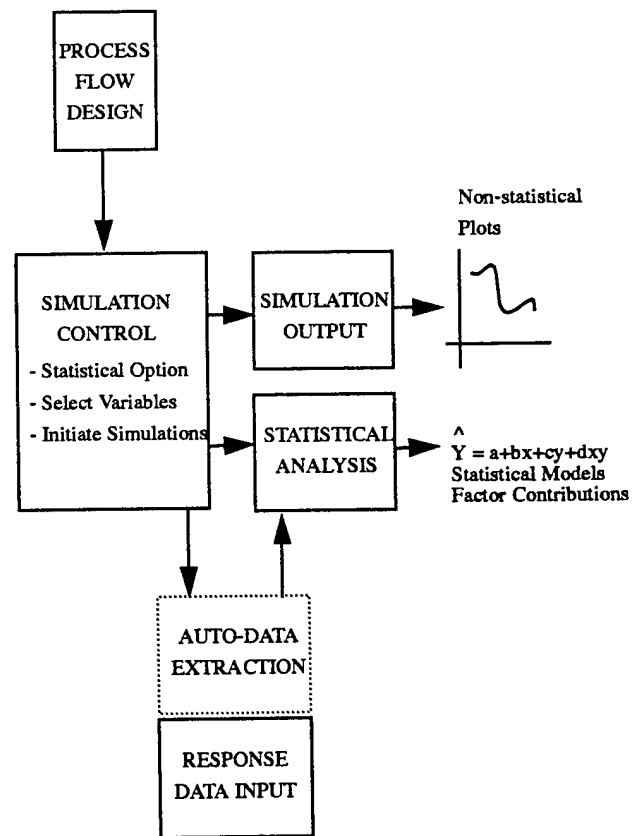

Fig. 4: STADIUM-SOI Main Menu

Fig. 5: STADIUM-SOI Block Diagram

A. Process Design

The Process Design module provides an easy-to-use interface designed to allow direct graphical creation of the process flow. The user need not look up, learn, or memorize any of the simulator-specific syntax. Process steps are selected (e.g. a button marked "Diffusion" is

pushed) and the flow is automatically built with the correct syntax. This minimizes the chance of error and subsequent computer crashes. Next, many of the decisions (e.g., model selection) that confront the inexperienced user are preset through the use of default values. Default decisions are made from careful examination of simulations of typical SOI device structures and the combined contributions from experienced users (semi-expert system). This includes the grid design. The user may simply allow STADIUM-SOI to generate a grid structure that is appropriate for statistical simulation.[3]

B. Simulation Control (DoE)

The Simulation Control module (Fig. 6) is the simulation experiment "desktop" with the following built-in statistical capabilities:

- Nominal Simulation
- Sensitivity Analysis
- Screening (Plackett-Burman)
- Fractional Factorial Designs
- Full Factorial Designs

Fig. 6: Simulation Control Menu

A nominal simulation is a single-run experiment with no input variation added. This single simulation run is used to determine if the device is valid. Next, variables are entered by selecting them (in a point & click fashion) in the simulation input file, entering the deviation (e.g. 1, 2, or 3 standard deviations or upper range), and assigning a name. Once the variables are established for a particular process, the appropriate statistical experiment design is selected. The selection displays the required runs and the level of modeling obtained for each particular choice. All of the information regarding the resulting model is dynamically provided in a clear format. In this way, the engineer is prompted to choose the experiment, not from a sophisticated knowledge of statistics, but rather based on the fundamental trade-off of runs (simulation time) vs. accuracy (model fit). Either the statistical standard deviation or the delta (= maximum value - mean) may be entered for the deviation. Simulations are run and the resulting data is analyzed. If the model is later found to be inadequate (based on R-squared value), the next level of experiment is chosen and a new DoE is generated.

C. Simulation Output

The Simulation Output module is used to extract and analyze non-statistical data for any previously run simulation (e.g., I-V plots, grid, contour structures, field lines, doping profiles, etc.).

D. Statistical Analysis

The Statistical Analysis module is divided into two functions: extraction and regression analysis. Data extraction collates the data and presents it in a form that is suitable for rapid identification and interpretation. Response variables are extracted and regression analysis performed by the statistical analysis module. The response variables that are automatically extracted are:

- Gate Oxide Thickness
- Peak Channel Doping
- Peak Source/Drain Doping
- Channel Length
- Transconductance
- Subthreshold Slope
- Breakdown Voltage

The regression analysis section derives a model for an output response, estimated mean, estimated standard deviation, and factor contributions. Again, the model is an equation comprised of statistically derived coefficients multiplied by the process and/or device variables (as identified by the experimenter).

IV. STADIUM-SOI Statistical Methods

A statistical experiment (often called an experimental design or design of experiment) consists of purposeful changes of the inputs (factors or variables) of a process in order to observe the corresponding changes in the outputs (responses). Thus, a statistical experiment is a scientific approach which allows the researcher to better understand a process and to determine how the inputs affect the responses.

One-factor-at-a-time experimentation or Monte Carlo methods, because of their simplicity, have often been used to predict the impact of factor variation on a response. These methods suffer from a number of related difficulties. The primary deficiency is that a large number of simulation runs are needed to obtain an accurate estimate and the estimate does not provide any additional information such as how the response varies as a function of input factors.

A carefully planned approach for conducting a statistical experiment, however, can give valid insight regarding how each factor affects the response. This statistical DoE methodology has been used successfully in actual manufacturing process development for many years.[4] It involves complex statistics and is often fully understood only by statisticians. STADIUM-SOI adopts this approach, handles the statistics internally, and provides an easy-to-understand procedure for performing statistical experiments through simulation.

The following sections are provided for those who desire a deeper understanding of the statistical foundation for STADIUM-SOI. However, only the most superficial understanding of these concepts is required to use the software effectively.

A. Nominal Simulation

The first step in STADIUM-SOI's systematic approach is the Nominal Simulation. As the name implies, all the input variables are set at their nominal, or mean value. STADIUM-SOI then performs a single simulation with the variables set at their nominal values. The purpose of the Nominal Simulation is to check the process for errors (i.e., the device characteristics match those expected).

B. Screening Experiment

Once the process has been successfully simulated with the factors set at their nominal levels, a screening experiment is performed. The purpose of screening is to reduce a large number of factors to a smaller set of important factors for subsequent experimentation. STADIUM-SOI uses Plackett-Burman[5] designs for its screening experiments. Plackett-Burman designs are based on Hadamard matrices where the number of runs in the matrix is a multiple of 4 (as opposed to powers of 2 for conventional designs). Designs of this type are advantageous, not only for their lower number of runs, but for their confounding patterns as well. Non-geometric Plackett-Burman designs, in which each two-factor interaction is partially confounded with each of the factors, provides the best measure of each factor's effect on the response in the least possible number of runs.[5]

The number of runs in a Plackett-Burman design is based on the number of factors. Table 4 describes the Plackett-Burman screening designs used in STADIUM-SOI.[5]

Table 4: Placket-Burman Screening Designs

FACTORS	RUNS
8 - 12	12
12 - 19	20
20 - 23	24
24 - 27	28
28 - 35	36

The purpose of screening is to identify those factors that affect the response. Heuristically, factors which contribute more than 5% to the variance of the response should be considered necessary and those which contribute less than 5% be considered "unimportant"[6].

C. Response Modeling

Once the important factors are identified the response modeling is performed. The goal of the modeling experiment is to mathematically relate the response to the input factors in the form of an equation. This model allows for the estimation of the response at levels other than those used in the experiment. This model is the basis upon which the estimated mean and variance of the response is calculated. The simplest form of a statistical model for 3 factors is:

$$\hat{Y} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_3 X_3 \qquad (1)$$

where β_n is a coefficient to be determined and the X_n represents the nth input factor. This equation relates the response, Y, to each of the factors. The symbol Y "hat" denotes that the response is "estimated". A more complex equation may be obtained by including "interaction terms".

Different modeling experiments yield different types of modeling equations. STADIUM-SOI automatically generates the appropriate modeling equation for each experiment.

Next, the two types of modeling experiments used, full factorial and fractional factorial, will be presented.

1. Full Factorial Experiment

The number of simulation runs for a full factorial design of k factors is 2^k. For example, a full factorial design for 3 factors requires 2^3 or 8 runs. One advantage of a full factorial experiment is the ability to produce a model that contains all possible interaction terms. The obvious disadvantage is the simulation time required to perform the experiment. Full factorial experiments become "expensive" quickly due to the relationship of the number of runs to the number of factors squared.

2. Fractional Factorial Experiment

Full factorial designs are often not feasible due to the lengthy durations involved in multiple process and device simulation. Running a design other than a full factorial can cause some interaction terms in the model to be lost. However, interactions with more than two-factors are seldom important. Therefore, fractional factorial designs can often be effectively implemented.

A fractional factorial design allows all of the factors and some of the interactions to be included in the model, while at the same time reducing the number of runs. As the name implies, a fractional factorial design is a fraction (or subset) of a full factorial design. The generation of these designs is often complicated and tedious, as there are many different fractional factorial designs possible for the same number of factors.

Instead of presenting the fractional factorial designs in terms of often confusing statistical jargon such as "resolution", "confounding", and "aliasing", STADIUM-SOI simply presents the selection in terms of the number of runs and takes care of the statistics internally.

D. Regression Analysis

To obtain models of the form shown in equation (1), STADIUM-SOI performs a classical regression analysis on the data. The model shown in (1) can be represented in an equivalent matrix form as shown below.

$$Y = X\beta \tag{2}$$

where

$$Y = \begin{bmatrix} y_1 \\ y_2 \\ y_3 \end{bmatrix} \tag{3}$$

$$X = \begin{bmatrix} 1 & X_1^1 & X_2^1 & X_3^1 \\ 1 & X_1^2 & X_2^2 & X_3^2 \\ 1 & X_1^3 & X_2^3 & X_3^3 \end{bmatrix} \tag{4}$$

and

$$\beta = \begin{bmatrix} \beta_0 \\ \beta_1 \\ \beta_2 \\ \beta_3 \end{bmatrix} \tag{5}$$

To determine $\bar{\beta}$ such that the least squares regression equation is solved:

$$\bar{\beta} = (X'X)^{-1}X'Y \tag{6}$$

to produce a regression model equation of the form shown in (1). A more generic form of (1) for n factors is:

$$\hat{Y} = \beta_0 + \sum_{i=1}^{n} \beta_i X_i \tag{7}$$

E. Estimated Mean and Variance

STADIUM-SOI uses (8) to estimate the response's mean. The mean values of each factor, $\bar{X}_i$, are substituted for the X_i's:

$$\hat{Y} = \beta_0 + \sum_{i=1}^{n} \beta_i \bar{X}_i \tag{8}$$

An estimate of the response's variance is obtained by using a first order Taylor expansion:

$$Var(Y) = \sum_{i=1}^{n} \left(\frac{d}{dX_i} \hat{Y} \right)^2 Var(X_i) \tag{9}$$

For the linear model the first order Taylor expansion yields the expression for the estimated variance of the response, Y:

$$Var(Y) = \sum_{i=1}^{n} \beta_i^2 Var(X_i) \tag{10}$$

F. Factor Contributions

In addition to the statistical model, estimated mean, and estimated variance, STADIUM-SOI calculates each factor's contribution to the variance of the

response. These factor contributions are used in screening to determine which factors are "important" in affecting the variability of the response. The contribution of factor X_i is calculated:

$$\text{Contribution of } X_i = \frac{\beta_i^2 Var(X_i)}{\sum\limits_{j=1}^{n} \beta_j^2 Var(X_j)} \qquad (11)$$

G. Model Fit

STADIUM-SOI gives an indication of how well the model predicts the data. This can also be thought of as how well or poorly the model and the data agree or "fit". The quantity is calculated:

$$R^2 = \frac{\sum\limits_{i=1}^{n} (\hat{Y}_j - \overline{Y})^2}{\sum\limits_{j=1}^{n} \left(Y_j - \overline{Y} \right)^2} \qquad (12)$$

R^2 is often referred to as the proportion of the variability in the data that is accounted for by the model. Clearly, the closer R^2 is to 1, the more response variation is accounted for and the model may be viewed as accurate.

V. Conclusion

It has been demonstrated that the understanding of the effect of process variation on device yield can be greatly improved through the application of DoE to process and device simulation. More important, the tools used to generate this data must be made viable through an intuitive user-friendly interface. Engineers will accept advanced simulation techniques only to the extent that they can be readily applied to a given situation. For this reason, STADIUM-SOI has been designed to enable process and device engineers to quickly and easily benefit from the powerful insight these modern TCAD tools and design of experiments can provide.

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[4] G. Smith, Statistical Process Control and Quality Improvement, Merrill, New York, 1991.

[5] Box, Hunter, and Hunter, Statistics for Experimenters, Wiley, Canada, 1978.

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Appendix F

**Biographical Sketches of the
AET, Inc. Staff
Who Worked on this Phase I SBIR Contract**

Thomas J. Sanders

Thomas J. Sanders is President of AET, Inc. He has over five years experience in directing software development research at Florida Institute of Technology. Since 1990, he has been Director of the Florida SEMATECH Center of Excellence. This center has received over $1.1 Million for work aimed at design for manufacturing, all of it managed by Dr. Sanders. The work of this center was rated as one of the three best achievements of all SEMATECH Centers of Excellence for all of 1993.

Dr. Sanders joined Florida Tech in 1989 as the Harris Professor of Electrical Engineering. He heads the Florida Tech microelectronics activities, is Director of the Florida Tech Electrical and Computer Science and Engineering Division, and was the Director of the Florida SEMATECH Center of Excellence. He continues to lead the research and development of the STADIUM statistical simulation methodology as he has since its inception. Prior to this time, he worked more than 20 years at Harris Semiconductor in Melbourne, Florida.

Dr. Sanders received a Doctor of Philosophy in Electrical Engineering from Purdue University in 1969. He immediately joined Harris Semiconductor as a device engineer and has held several engineering management positions, including a promotion in 1982 to Vice President of Engineering with responsibilities for process and product design.

Dr. Sanders is a Fellow of the IEEE and has been a member of the Board of Directors for SRC. He has been on the technical advisory boards of SEMATECH and the Microelectronics and Computer Technology Corporation and has been active in the CFI TCAD Framework Initiative. Dr. Sanders holds 11 patents and is the author of more than 35 technical papers. He holds memberships in Tau Beta PI, Eta Kappa Nu and Sigma Xi.

A bibliography of several recent papers written by Dr. Sanders which reflect the breath and depth of his competence in this area are presented in the References section.

Mark J. Phelps

Mark J. Phelps is currently a research and development engineer for AET, Inc. He has over 8 years of experience in the field of electronics and will receive a Ph.D. degree in electrical engineering in December 1995. Mr. Phelps also holds Master's and Bachelor's degrees in electrical engineering and graduated Summa Cum Laude. His research interests include process, device, and circuit modeling of Silicon-On-Insulator (SOI) devices and the development of statistical TCAD design tools. His current work involves extensive study of SOI device physics and the implementation of new and existing models into computer simulation software.

Mr. Phelps was the lead engineer for a software shell called STADIUM-SOI that applies statistics to process and device simulators (SUPREM & PISCES) for SOI devices. This project was written in the C programming language for use in UNIX, SunOS, and Openwindows environments. Mr. Phelps has performed statistical device modeling using Design-Of-Experiments (DOE) and linear regression analysis of low-power SOI MOSFETs which were partially & fully-depleted. MOS devices from 0.5u to deep sub-micron were investigated, developed, and simulated to determine feasibility as low power devices. Mr. Phelps is a co-author of 6 papers in the areas of statistical device modeling and characterization through computer simulation.

Prior to coming to AET, Mr. Phelps worked for three years as a research engineer through Florida Tech for SRC, SEMATECH, and Texas Instruments. During this time, he designed algorithms and software for a statistical design-of-experiments based multiple simulation shell which involved the creation of graphical-user-interface windows and C programming. Other tasks included the investigation, simulation, and development of Built-In-Lateral-Isolation (BILI) CMOS process, the design and coding of automated gridding (mesh) techniques for use in computer simulation, and the development of data extraction and scientific data visualization routines for a Forward Looking Infrared device simulation program (FLIR90).

From 1986-1990, Mr. Phelps was an electronics technician, second class petty officer, in the United States Coast Guard. His responsibilities included maintenance and repair of all station and shipboard electronics including UHF and VHF transceivers and X-band radar systems. During his enlistment he was honored with an appointment to Officer of the Day (acting Commanding Officer in his absence) and received an honorable discharge in 1990.

Glenn T. Hess

Glenn T. Hess is an electrical engineering Ph.D. candidate at the Florida Institute of Technology working under Dr.Thomas Sanders in the area of statistical optimization and simulation. He has worked on the development of STADIUM's statistical capabilities and is presently working on his dissertation which involves applying optimization techniques to simulation environments. His technical background is in semiconductor device physics and statistics. He currently teaches undergraduate semiconductor device theory and has three publications to his credit.

Mr. Hess received has Bachelor of Science in electrical engineering from the University of Florida in 1990. His primary area of study was semiconductor device theory and the development of Silicon-Germanium strained layers. He completed his Master of Science in electrical engineering from the Florida Institute of Technology in 1993 where he was employed as a research assistant. His research included the fabrication of multi-chip modules, the characterization and optimization of PECVD Silicon Nitride films, as well as statistical process and device simulation. His thesis involved the statistical process and device simulation of a rad-hard SOI bipolar process and was funded by Texas Instruments.

Mr. Hess has industry experience with Storage Technology Corporation where he developed failure analysis techniques for photoconductors and performed reliability modeling on laser printer sub-systems. He was also employed by Harris Semiconductor where he developed a technique for predicting device performance based on the characterization of starting SOI material.

Dale P. Means

Dale P. Means joined Florida Tech as a Research Associate in 1989. During this time he has managed the STADIUM software development for the Florida SEMATECH Center of Excellence, designed the architecture and flow of this software, and provided guidance for the graduate students working on the project. Mr. Means also has responsibilities for the management and system administration of the Sun UNIX computing resources for the Electrical and Computer Engineering Department at Florida Tech. Prior to joining Florida Tech, Mr. Means worked as a software engineer for Harris Corporation for 10 years. Mr. Means has 25 years of software development experience, with nearly 20 of that in engineering areas. Mr. Means received a Bachelor of Science degree from Florida State University in 1966.

The bibliography at the end of this proposal includes many papers authored or co-authored by Mr. Means which are directly related to the STADIUM statistical simulation methodology.

Thomas J. Sanders, Jr.

Tom Sanders has been with AET, Inc. since March 1994, working as the Operations Manager. He also serves as an Officer of the Corporation under the titles of Secretary and Treasurer. His main duties include keeping the accounting records for the company, assisting with marketing and sales, and handling all of the general and administrative tasks for the company.

Mr. Sanders holds a Bachelor of Science degree in Business Administration (with an emphasis in Marketing) from the University of Florida. He also has recently attained a Masters in Business Administration (MBA) from Florida Tech. Prior to working with AET, Mr. Sanders was employed by Harris Semiconductor (Melbourne, Florida) as an Associate Tactical Marketing Administrator. Most of his responsibility was in the area of market research for several of the product lines at Harris. Mr. Sanders has also been employed as an Account Executive for Southern Cellular Telecom (Melbourne, Florida). His responsibilities included marketing and selling cellular telephones and long distance telephone service to companies in the city of Melbourne.

Jacob A. Davis

Dr. Jacob A. Davis is Vice President of Business Planning and Finance for AET, Inc. and is Visiting Professor in Engineering Management at Florida Institute of Technology. Prior to joining AET, Dr. Davis was with Harris Semiconductor for 26 years. During the last 12 years with Harris Semiconductor, he was Vice President-General Manager of the Military and Aerospace Division, the Custom Integrated Circuits Division and the Harris Microwave Division. Dr. Davis has served in a variety of other capacities at Harris Semiconductor including Vice President of Engineering, Director of Manufacturing, Director of Special Services, and Device Research Engineer.

Dr. Davis received a Doctor of Philosophy from Purdue University in 1969 and a Bachelors of Science in Electrical Engineering from North Carolina State University. After graduation from Purdue, Dr. Davis joined Harris Semiconductor as a Device Research Engineer involved the design and production of integrated circuits. He is a Member of the IEEE and the Electrochemical Society, and has served on a variety of advisory boards for several Universities. He holds four patents and has given a number of overview and invited papers at several conferences. He is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Pi Sigma, Phi Kappa Phi, Pi Mu Epsilon and Sigma Xi.

Bob G. Quinn

Bob G. Quinn is the Vice President of Business Development for AET and is one of the co-founders of the company. Prior to joining AET, Mr. Quinn was with Harris Semiconductor for 12 years where he held positions as VP of Marketing and Sales and Manager of Business Development. In these positions he managed, developed and implemented marketing, sales, and contract pursuit activities for major strategic programs for the Military and Aerospace Division via many government agencies. He also managed contract administration, press relations, market communications and strategic marketing functions. During this time annual orders increased from $35 million in 1982 to $190 million in 1989, making Harris the number one worldwide supplier to the military aerospace industry. Prior to joining Harris, Mr. Quinn was employed by Texas Instruments where he progressed from silicon transistor manufacturing engineer to sector government accounts marketing manager. Intermediate positions included silicon transistor marketing manager, Minuteman missile program manager and digital IC military product marketing manager. Mr. Quinn served as the company representative to the EIA Solid State JEDEC Council for two years. He received a B.S. in Electrical Engineering from Mississippi State University. He is a member of IEEE and Armed Forces Communications & Electronics Association.